SOLID FADC test status and plan

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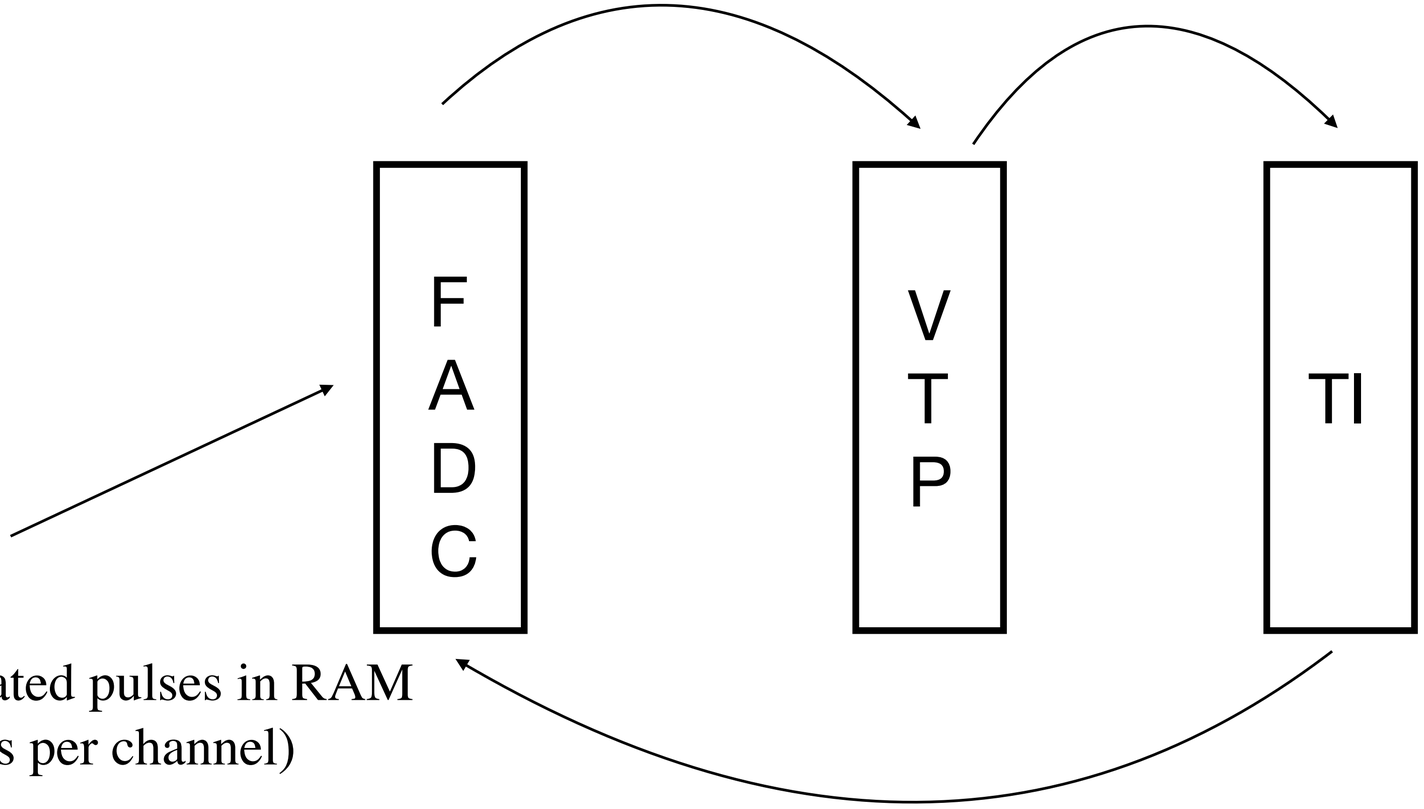
Test stand setup

compton firmware: generate trigger when there is a signal in FADC channel 0

Trigger_1: send a trigger to TI to read out FADC data



playback:
save simulated pulses in RAM
(32 samples per channel)

Trigger_2: TI internal pulser generates a Trigger_2 type trigger which injects the simulated data in the FADC

(Event rate can be controlled here)

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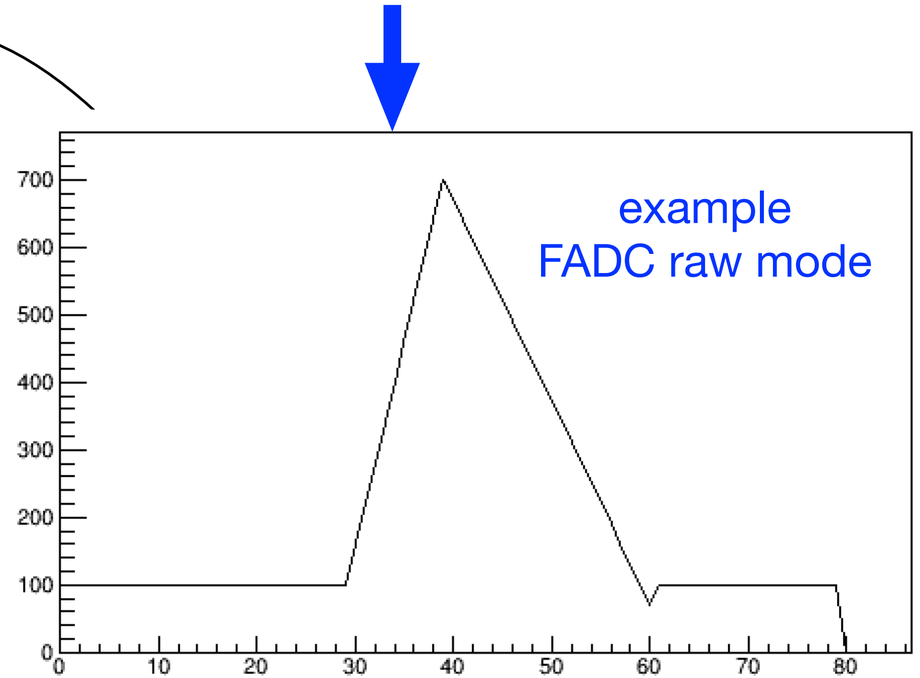

FADC

VTP

playback:
save simulated pulses in RAM (32 samples per channel)

Trigger_2: TI internal pulser generates a Trigger_2 type trigger which injects the simulated data in the FADC

(Event rate can be controlled here;
rate = 500kHz/2^n, n=0-15)

FADC dead time measurement plan

- Ben is going to update the FADC firmware to allow part of the FADC channels can accept analog input
- Send MPS signals from the helicity board to FADC so the scalers in VTP can be enabled
- With 16 FADC channels enabled, set the random pulser rate (500kHz/2^n) to:
  - n=8, rate = 1.95 kHz
  - n=6, rate = 7.81 kHz
  - n=5, rate = 15.625 kHz
  - n=4, rate = 31.25 kHz
  - n=3, rate = 62.5 kHz
  - n=2, rate = 125 kHz
  - n=1, rate = 250 kHz
- Measure the FADC dead time as (1 - FADC_counts/scaler_counts)