SOLID FADC test dead time measurement

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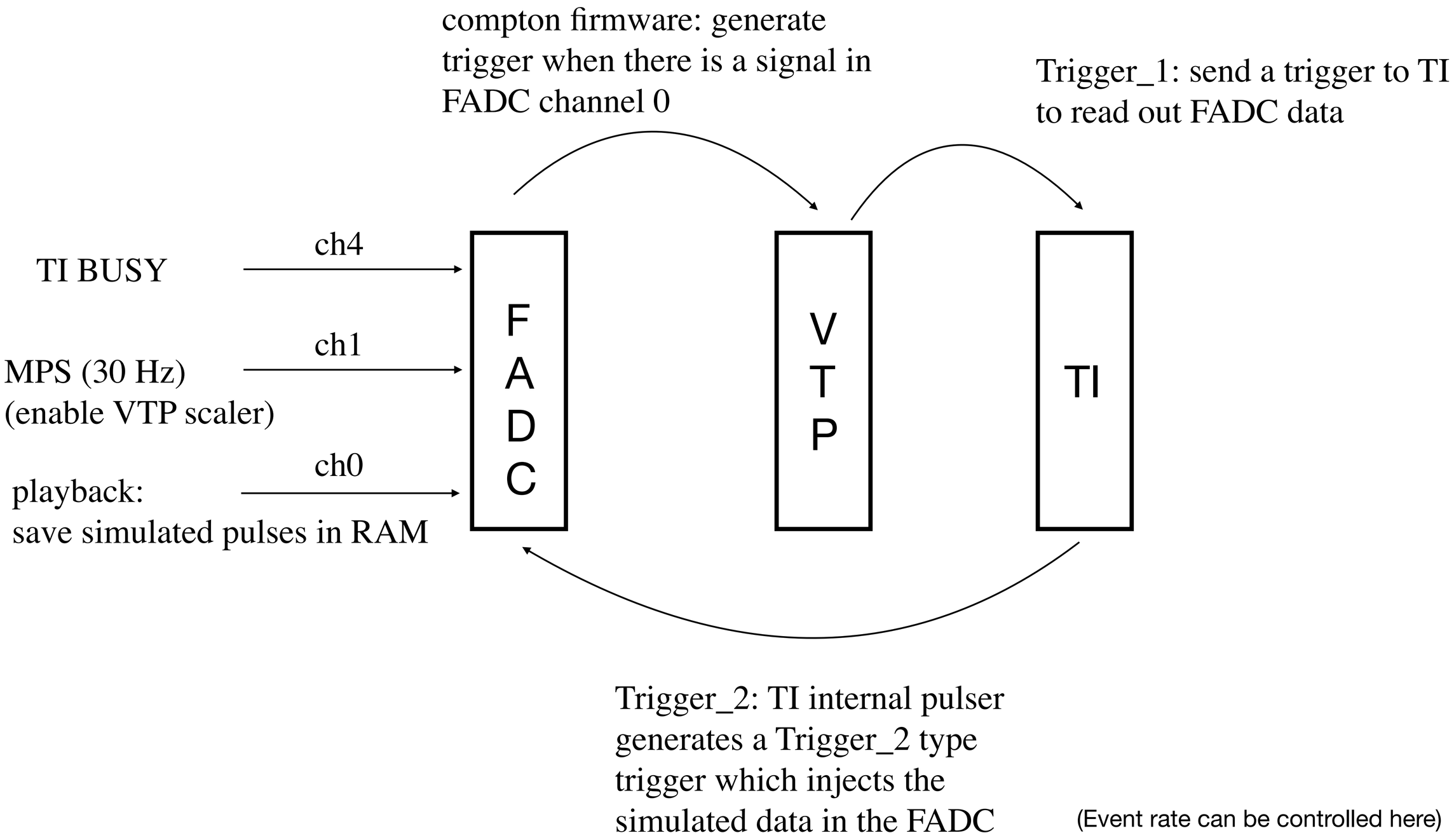

compton firmware: generate trigger when there is a signal in FADC channel 0
Trigger_1: send a trigger to TI to read out FADC data
TI BUSY
ch4
MPS (30 Hz)
(enable VTP scaler)
ch1
playback:
save simulated pulses in RAM
ch0
FADC
VTP
TI
Trigger_2: TI internal pulser generates a Trigger_2 type trigger which injects the simulated data in the FADC
(Event rate can be controlled here)

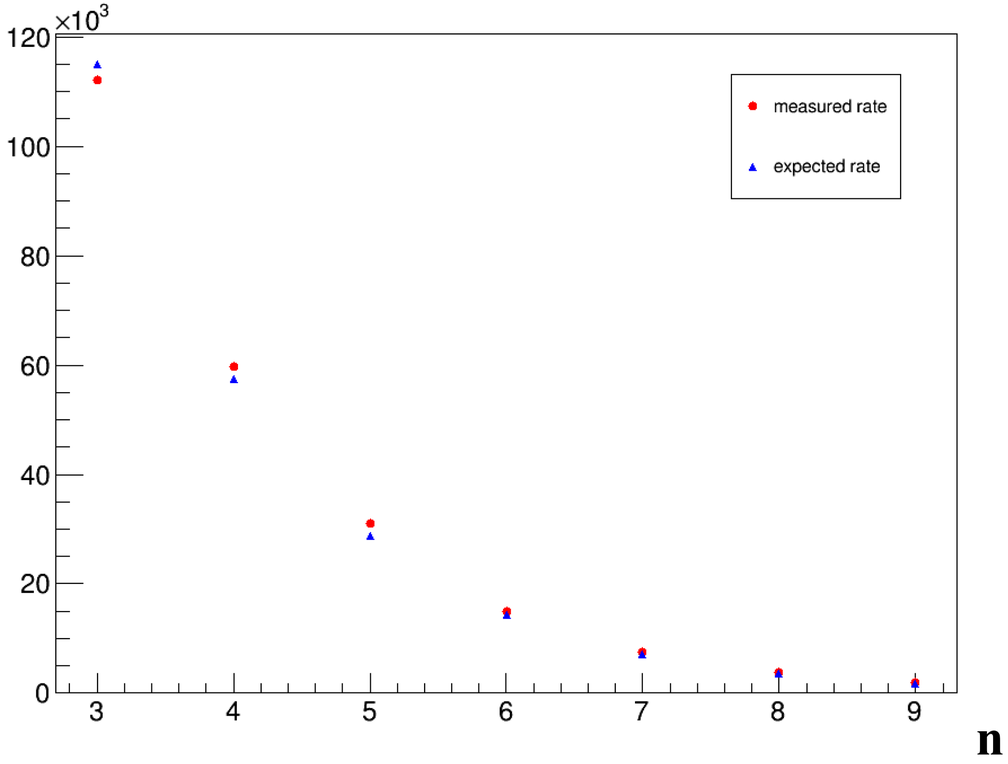
Dead time results

Blocklevel=10 , bufferlevel=10

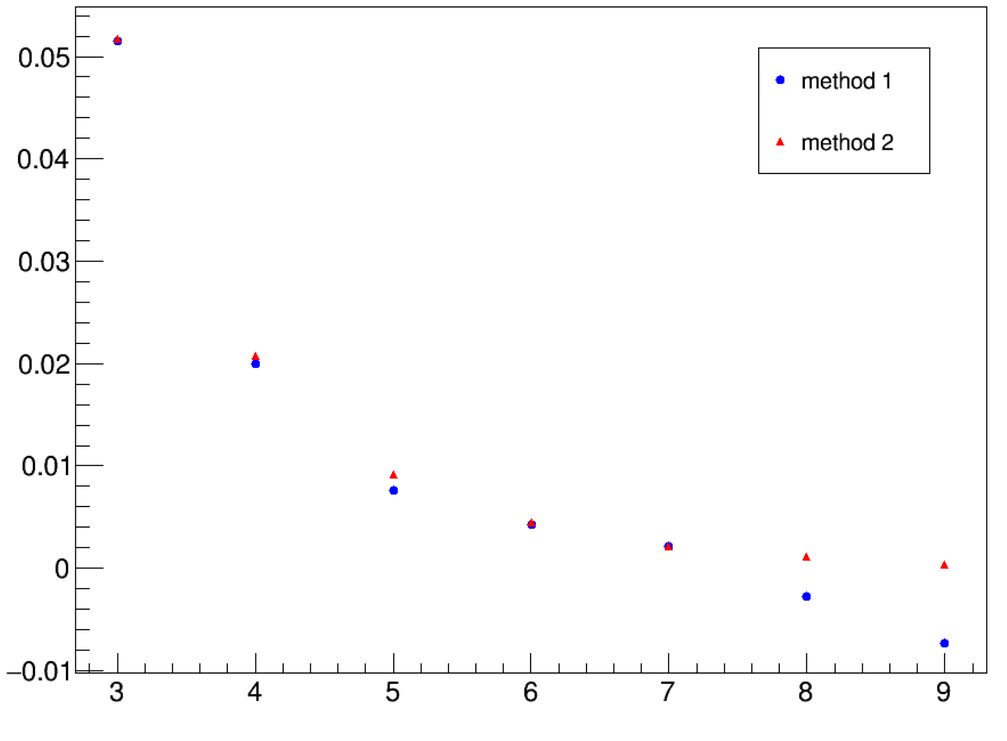
1. Random pulser with 3 FADC channels enabled (1 channels has the playback input)
   trigger rate = 460 kHz/2^(n-1) (n=9, 8, 7, 6, 5, 4, 3)

2. method 1: dt = 1 - fadc_real_counts/fadc_scaler_counts:
   fadc_real_counts: the total number of events with fadc_a[0]>0
   method 2: dt = 1 - trigger_counts/fadc_scaler_counts

event rate (Hz)



Dead time

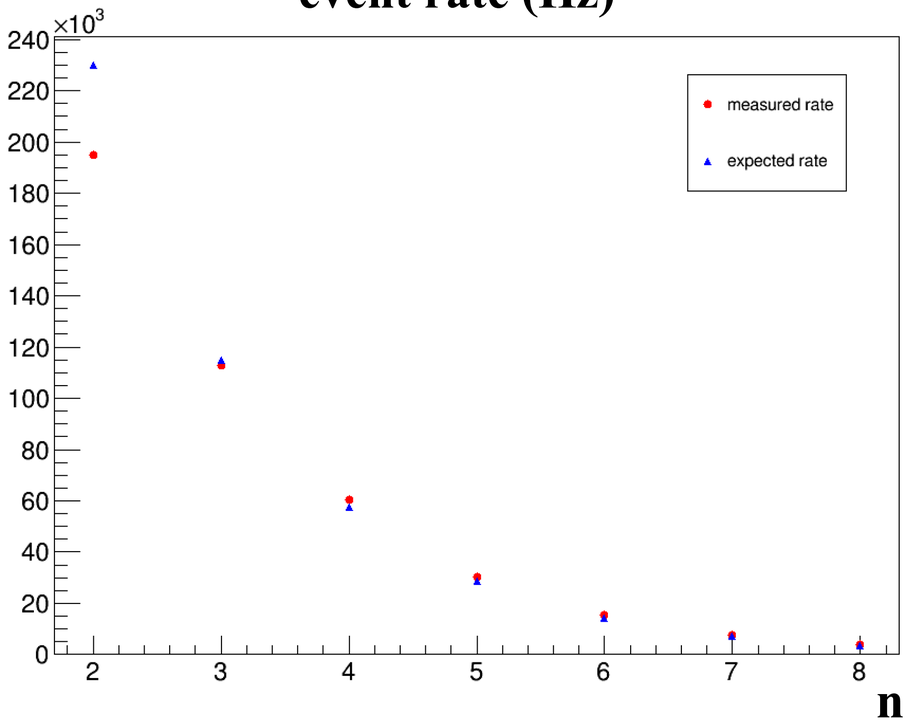


Dead time results

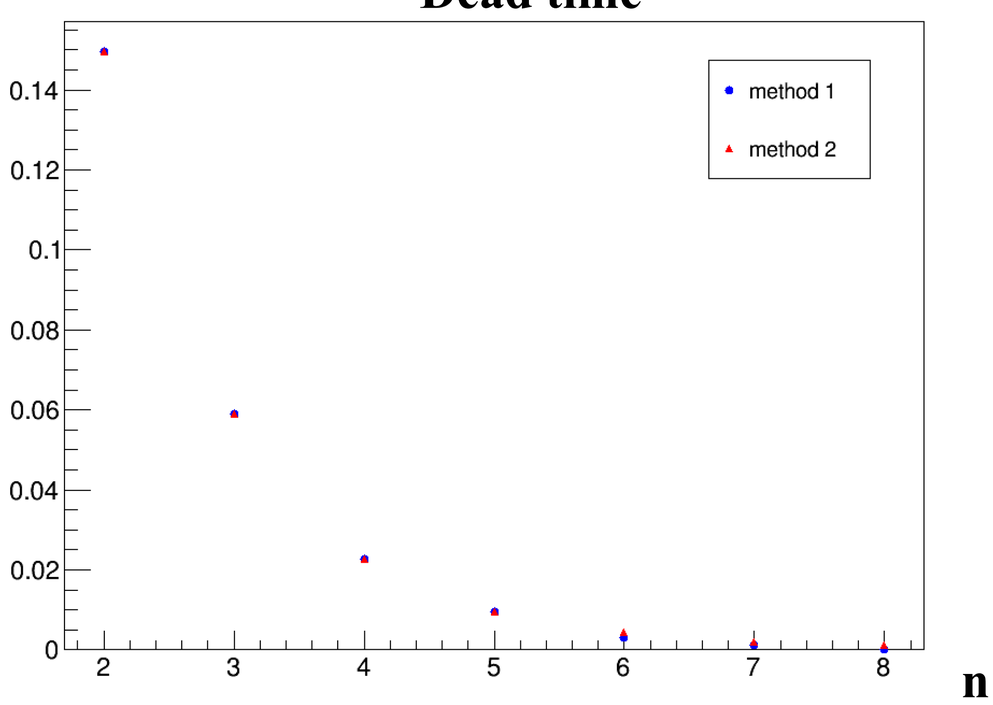
Blocklevel=10 , bufferlevel=10

1. Random pulser with all FADC channels enabled (14 channels have the playback input)
   trigger rate = 460 kHz/2^(n-1) (n=8, 7, 6, 5, 4, 3, 2)

event rate (Hz)



Dead time



- Increasing to Blocklevel=20 and bufferlevel=20 doesn't change the dead time;
- At blocklevel=25 and bufferlevel=25, get warnings in CODA:
  jlabTsi148DmaSend: WARN: Specified number of DMA bytes (66088) is greater than
  the space left in the buffer (60908). Using 60908
- Next step: generate a small asymmetry and measure the asymmetry ——> how to generate a small asymmetry?