

SOLID FADC test dead time measurement

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compton firmware: generate trigger when there is a signal in FADC channel 0

Trigger_1: send a trigger to TI to read out FADC data

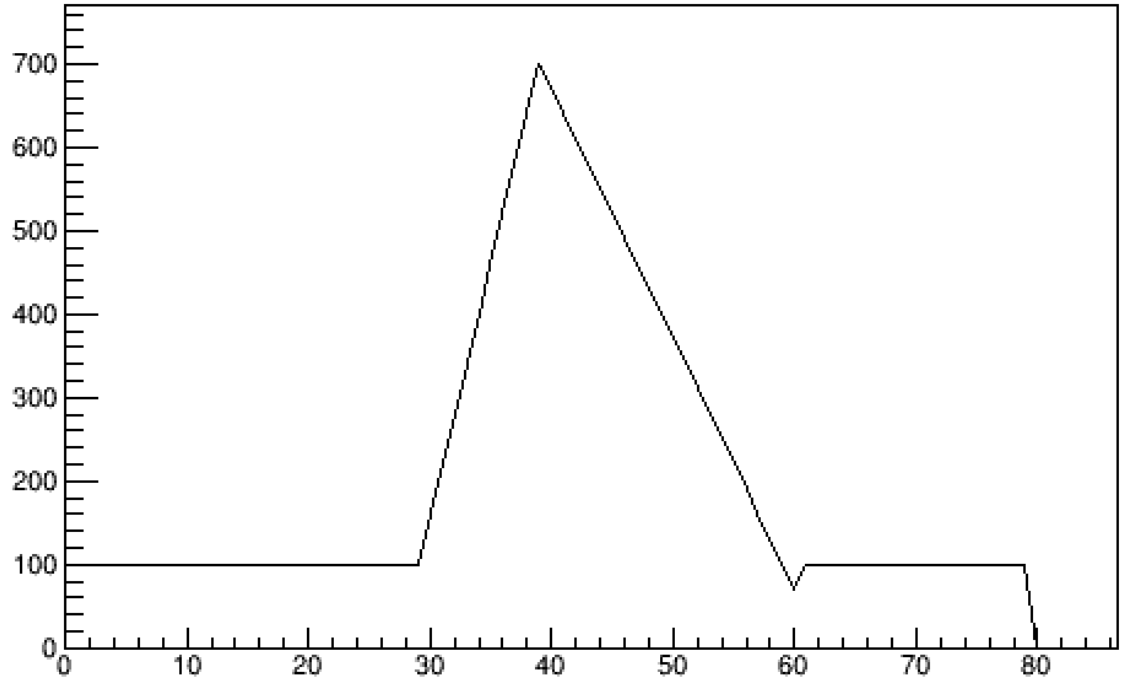
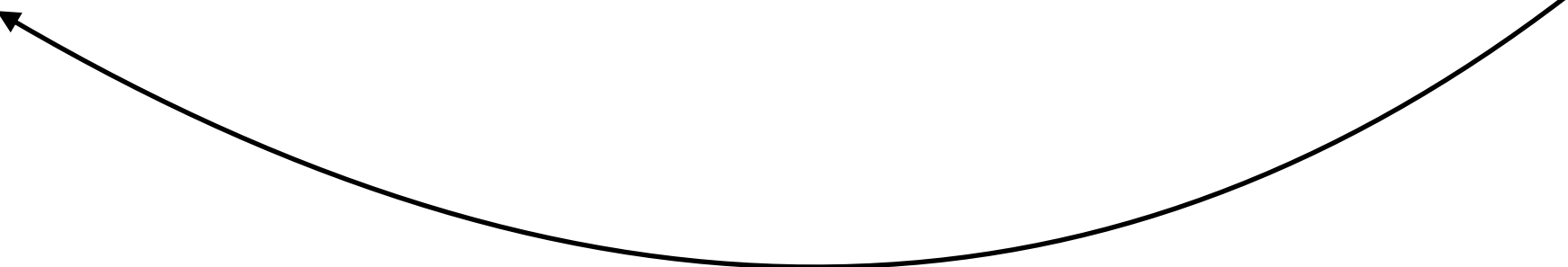
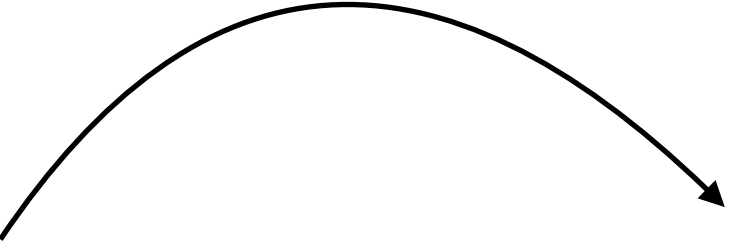
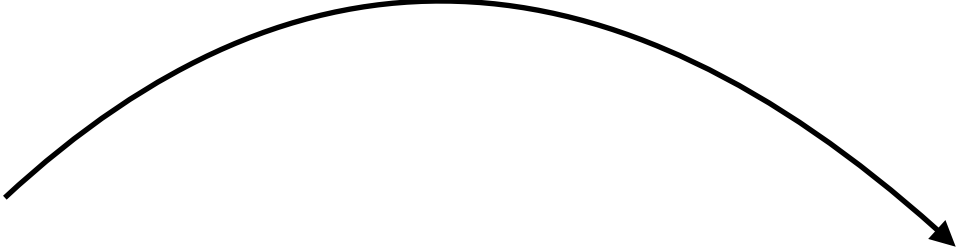
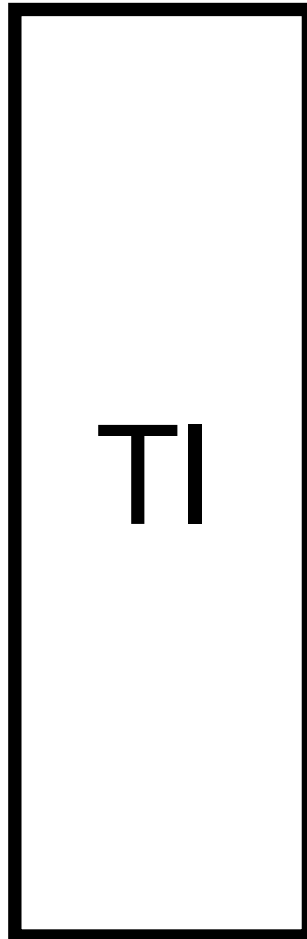
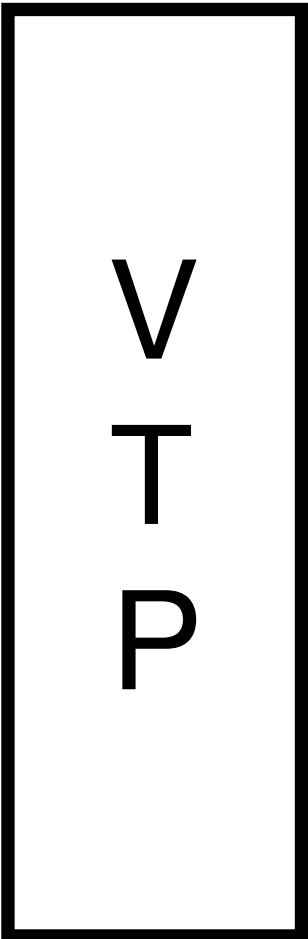
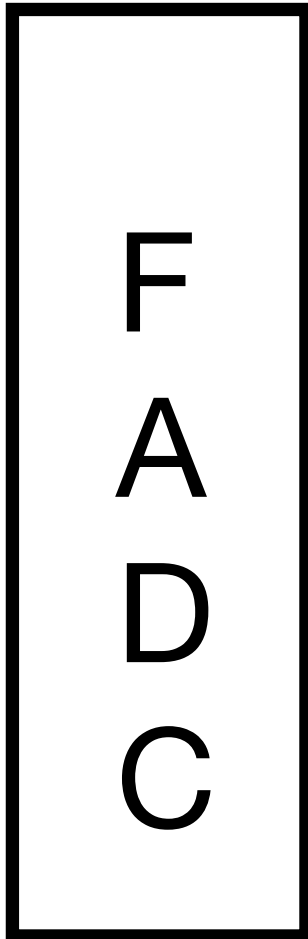
MPS (30 Hz)
(enable VTP scaler)

ch1



playback:
save simulated pulses in RAM

ch0

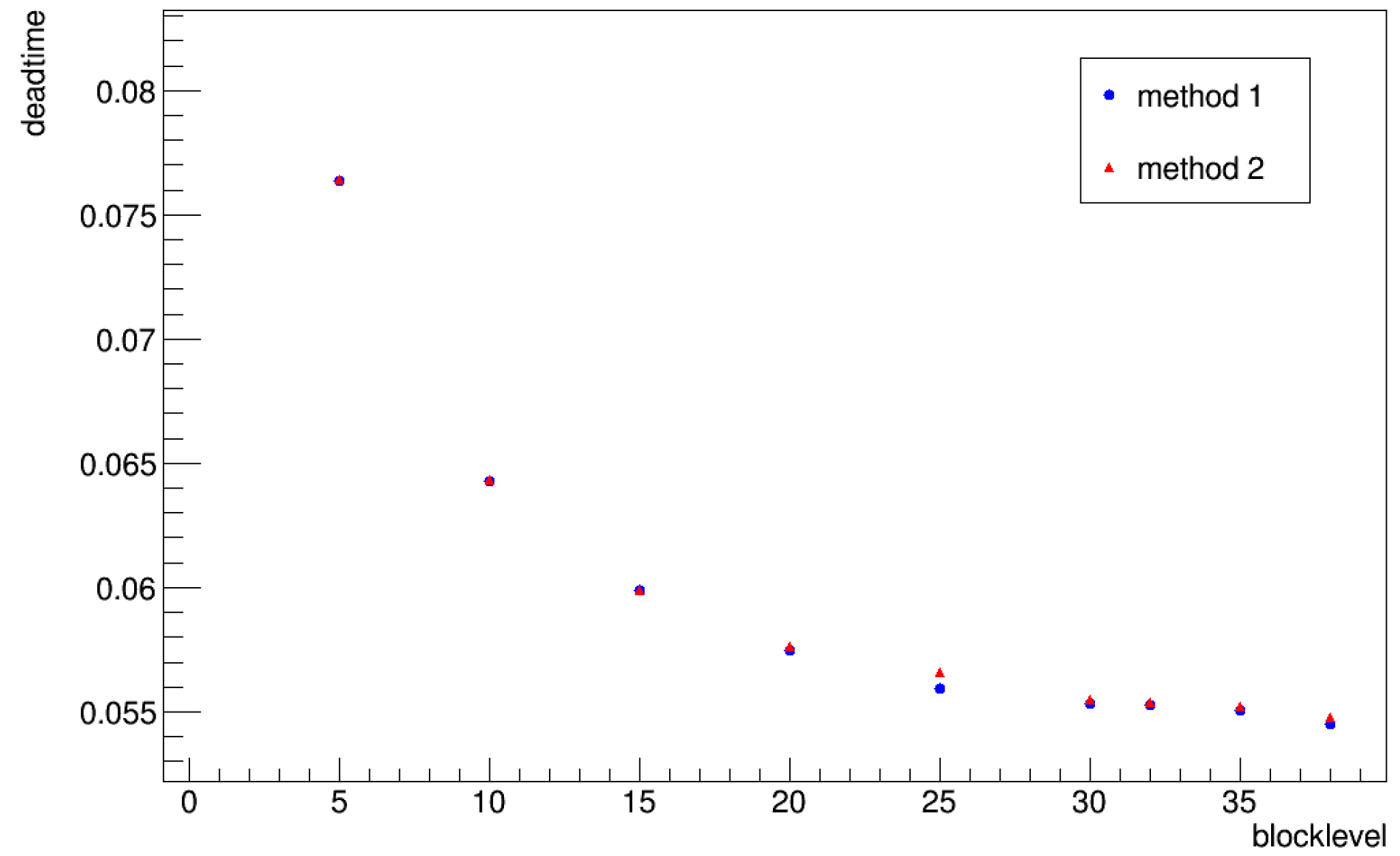
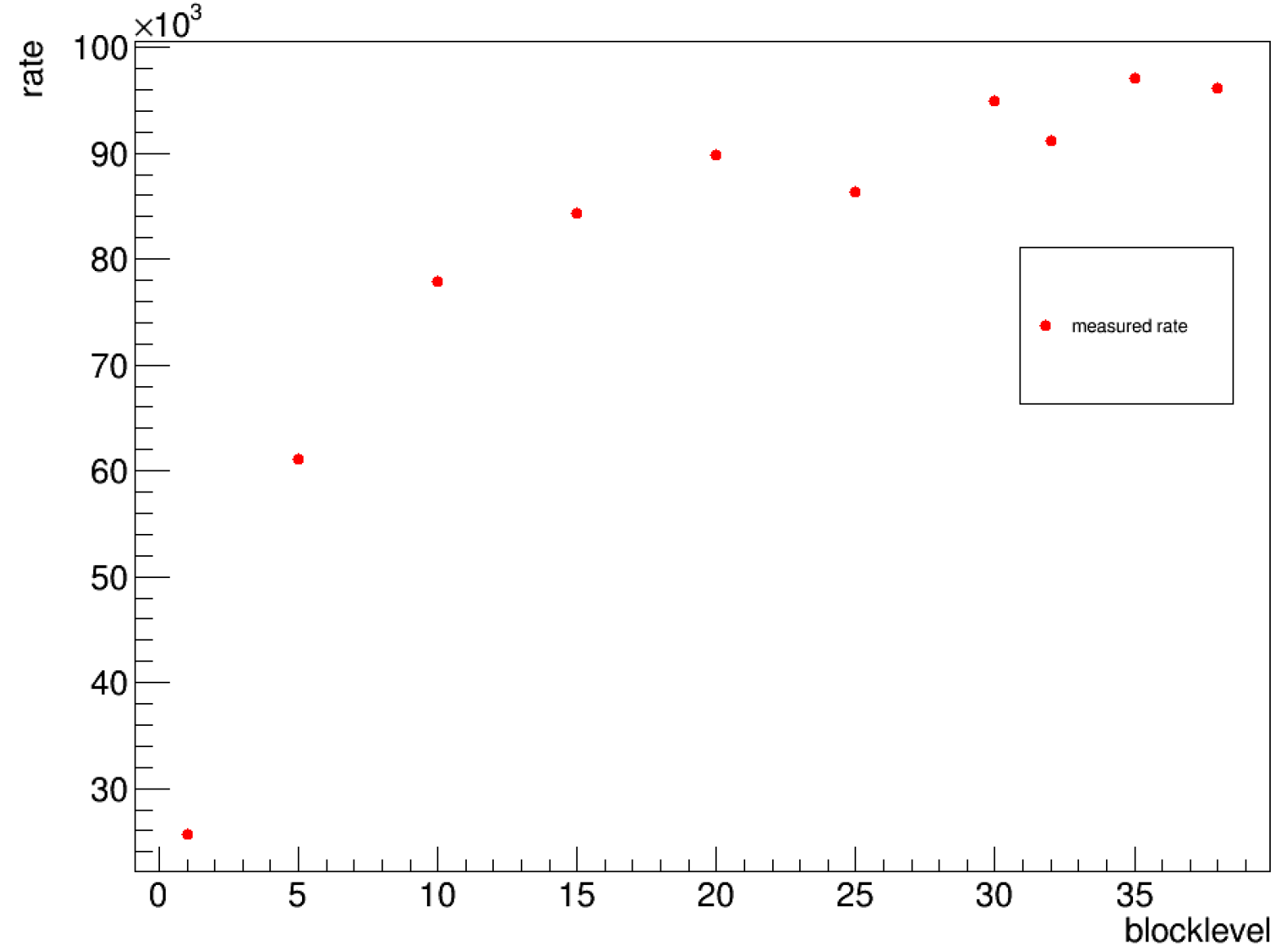


Trigger_2: TI internal pulser generates a Trigger_2 type trigger which injects the simulated data in the FADC

(Event rate can be controlled here)

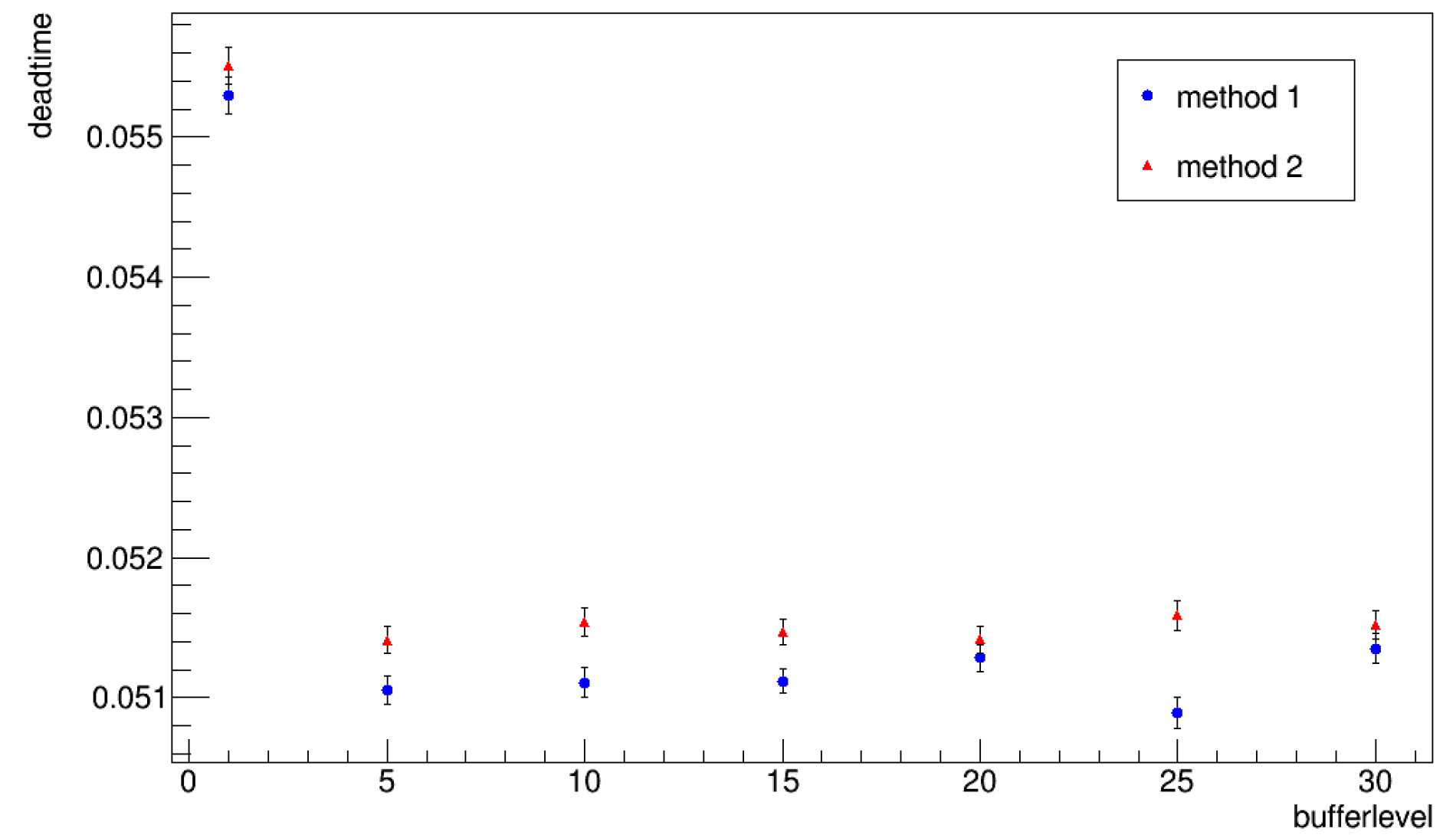
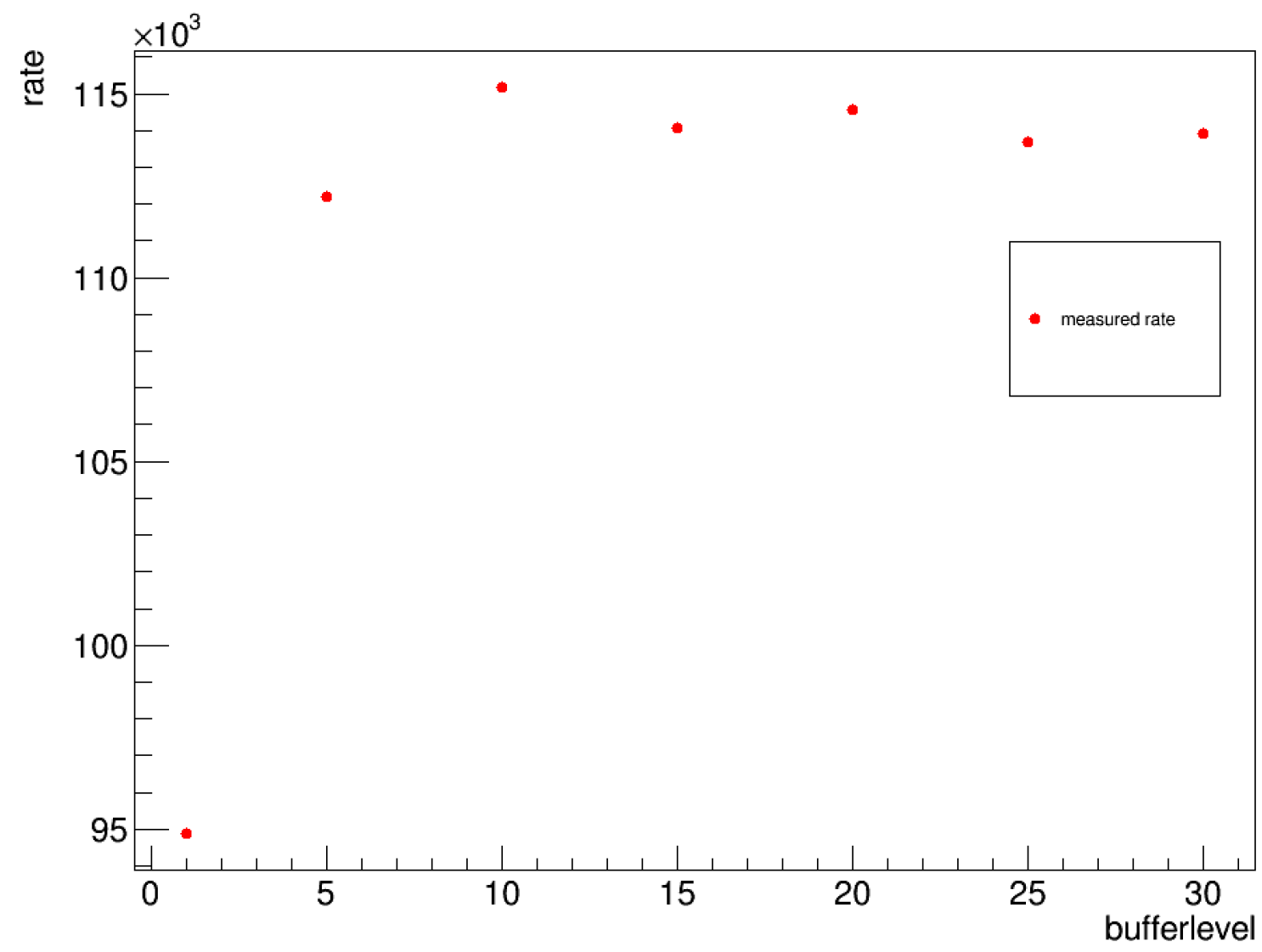
Decide Blocklevel and Bufferlevel for integral mode (mode 3)

1. Keep bufferlevel=1. increase block level until the “data rate” and “event rate” saturate.



choose:
Blocklevel=30

2. Keep blocklevel=30, increase buffer level and check the dead time

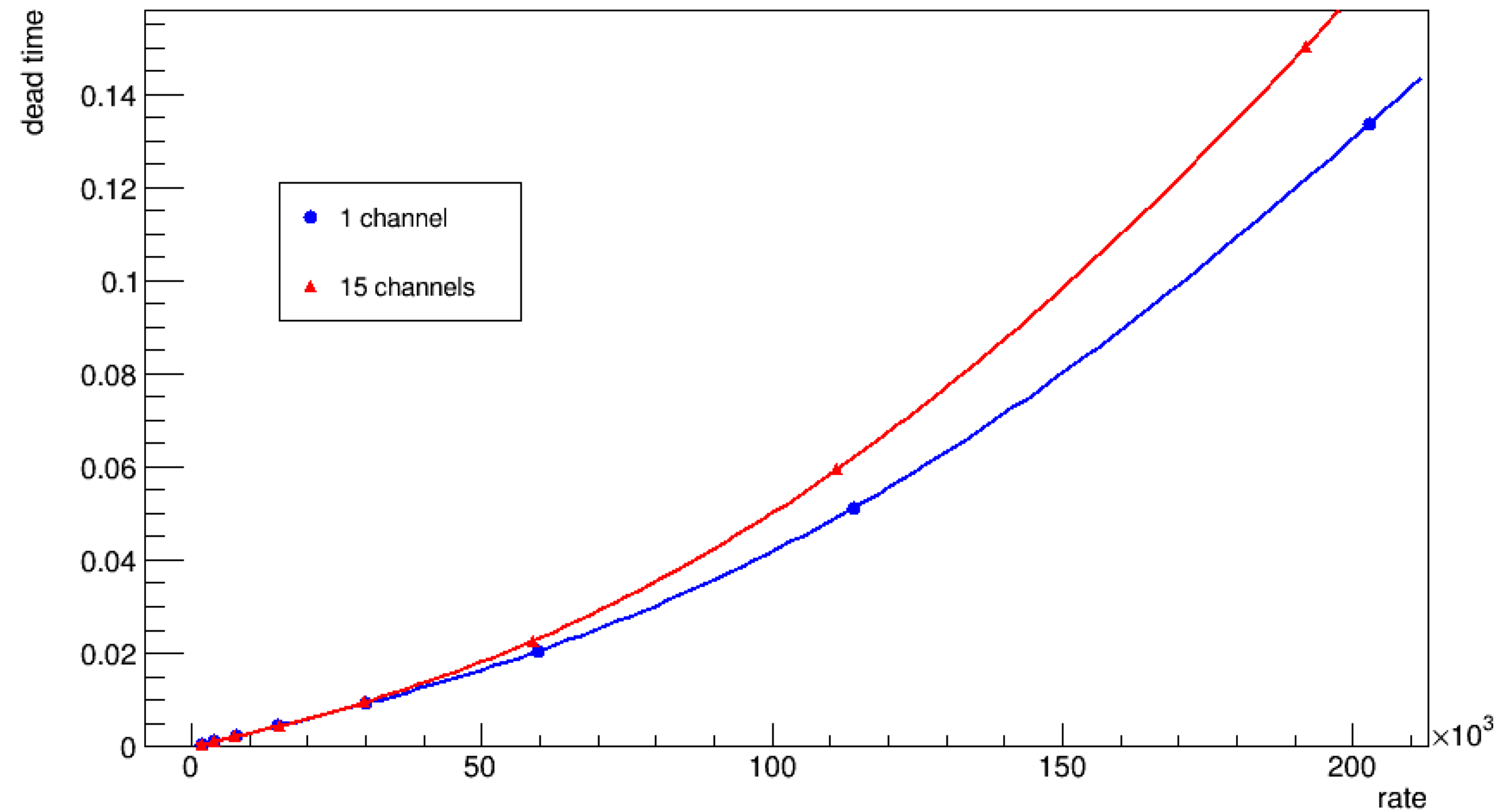


choose:
Bufferlevel=10

Dead time for integral mode (mode 3)

dead time = $1 - \text{trigger_counts}/\text{fadc_scaler_counts}$

(trigger counts are enabled the same time as the fadc scaler counts)



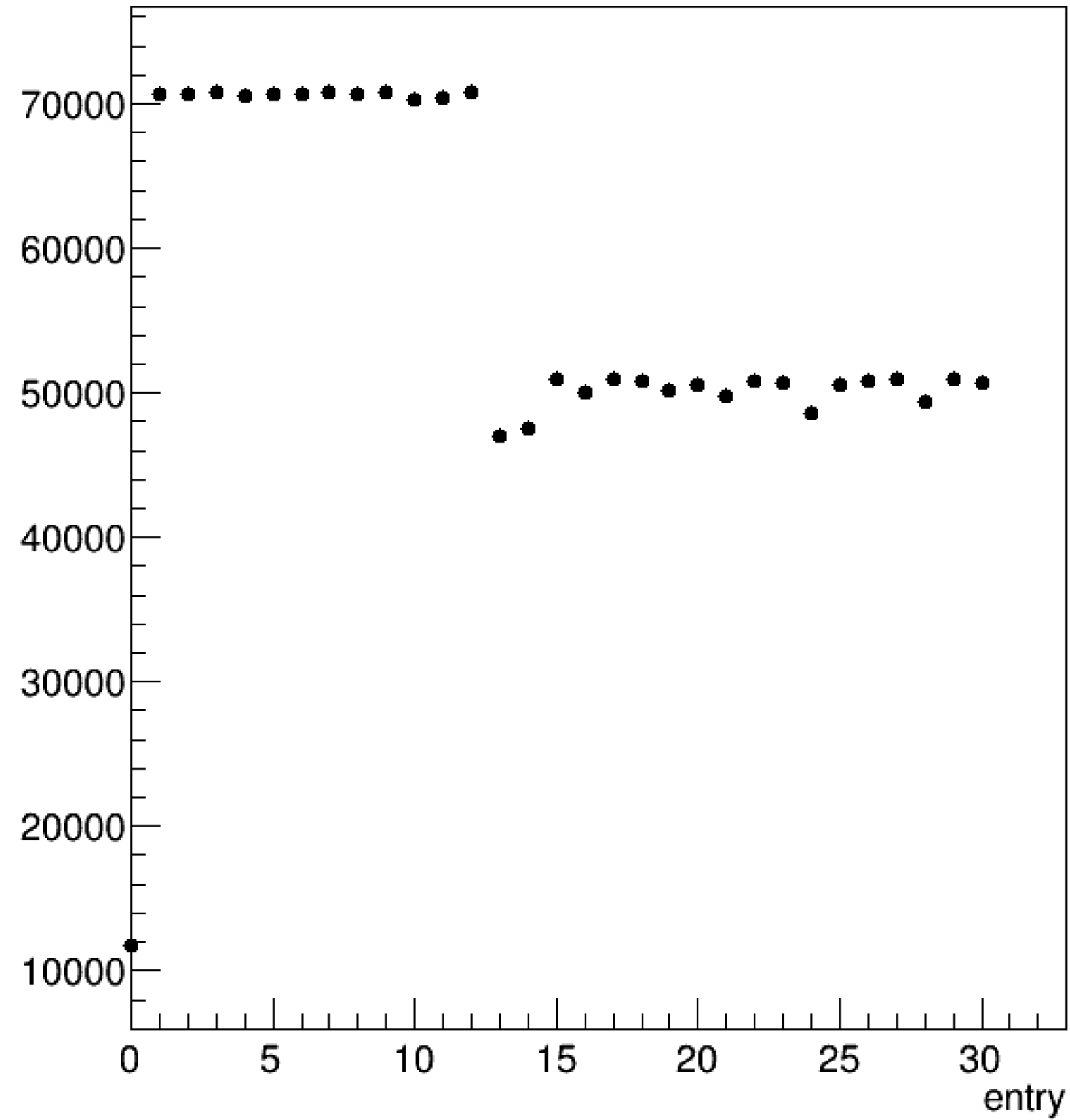
```
***** 1 channel pol4 function *****
Minimizer is Linear / Migrad
Chi2          =      0.919621
Ndf           =           3
p0            = -6.25314e-05 +/- 6.17749e-05
p1            =  2.93322e-07 +/- 9.95843e-09
p2            =  6.3317e-14  +/- 3.11513e-13
p3            =  1.52092e-17 +/- 2.9814e-18
p4            = -3.27372e-23 +/- 8.29944e-24
```

```
***** 15 channel pol4 function *****
Minimizer is Linear / Migrad
Chi2          =      0.854604
Ndf           =           3
p0            =  4.72116e-05 +/- 5.48128e-05
p1            =  2.65675e-07 +/- 8.70978e-09
p2            =  1.38717e-12 +/- 2.82815e-13
p3            =  1.2639e-17  +/- 2.83388e-18
p4            = -3.04538e-23 +/- 8.30375e-24
```

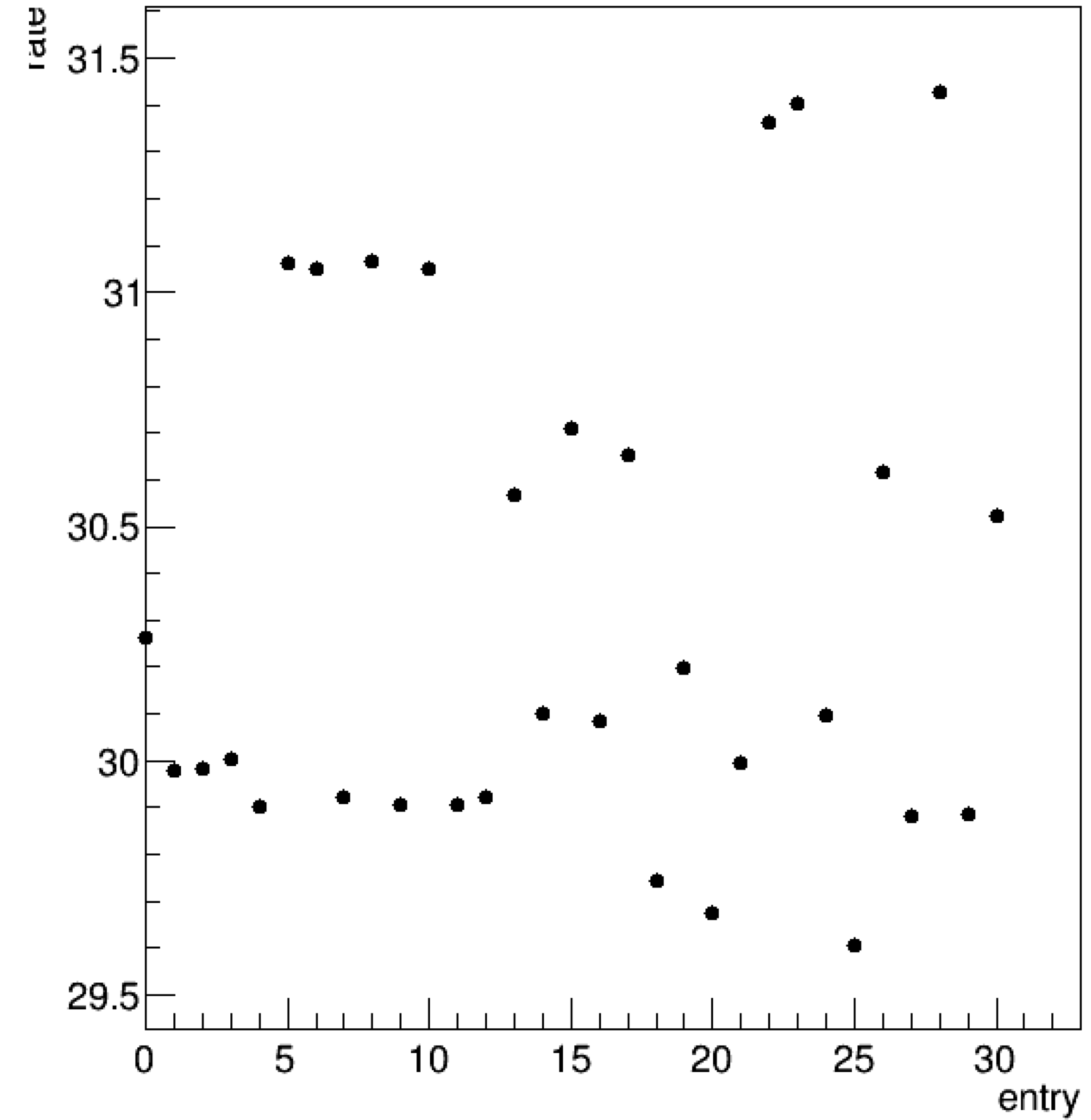
Decide Blocklevel and Bufferlevel for raw mode (mode 1)

Blocklevel=35, Bufferlevel=10

Chan0 rate



Chan1 rate



Rate changes during the run?