SoLID VMM3 prototype board power

In order to simplify the prototype design, power for the components will be supplied from a mezzanine card. This allow us to defer detailed design of the power circuitry until later. A power mezzanine with COTS components can be initially used, being replaced in the future with a radiation tolerant design (FEAST based). The basic concept is shown in the following two figures.

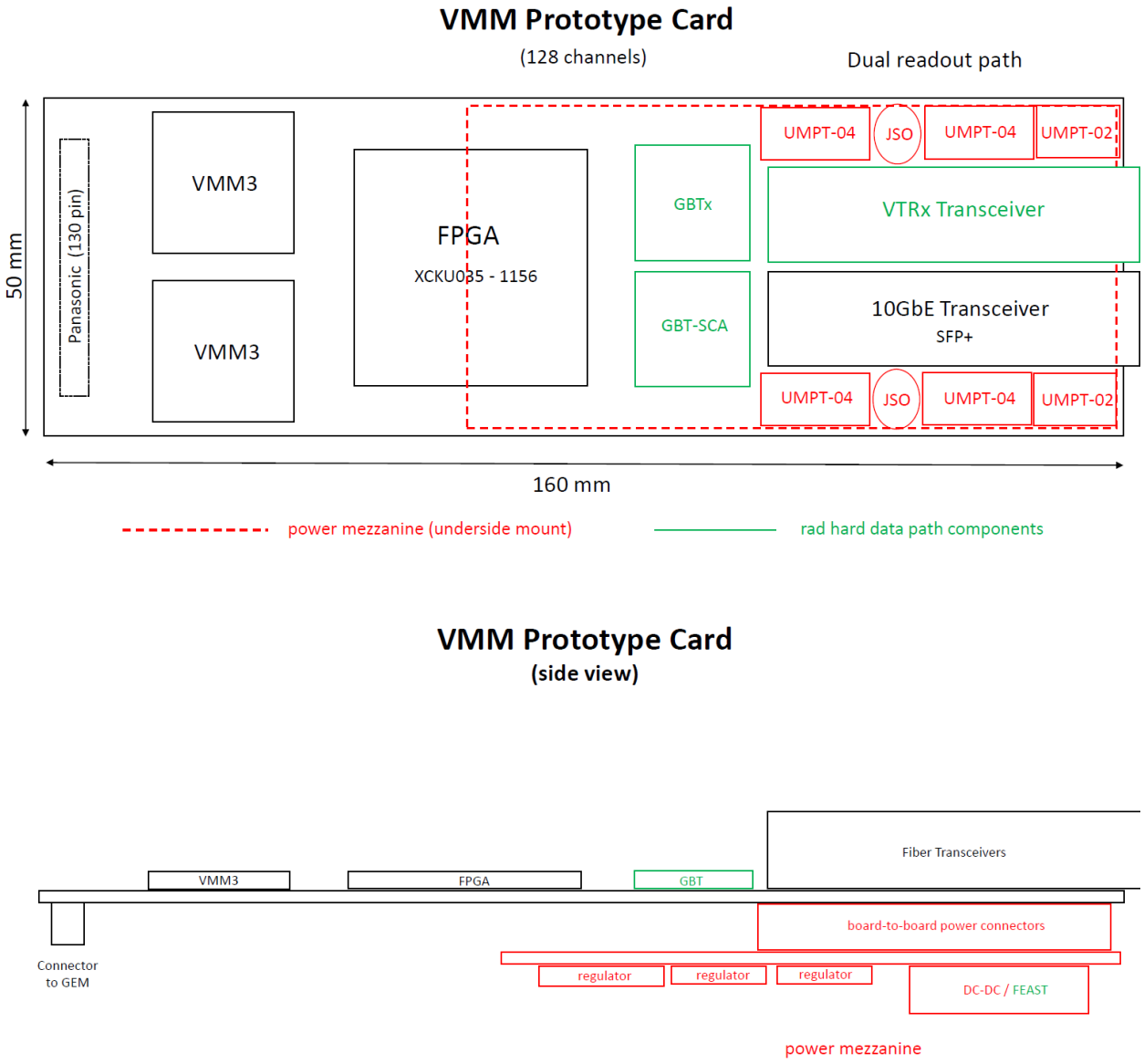

Figure 1. Power Mezzanine concept for VMM Prototype Card

VMM ASIC power

There are 4 voltages to supply to the VMM3: Vddp (analog), Vdd (analog), Vddad (mixed), Vddd (digital) (all nominal 1.2V)

Three existing designs using the VMM3 were looked at:

GPVMM3 Evaluation board. Design has a single VMM chip. Each power rail for it is supplied with an independent regulator. This is the ideal case. The lowest noise will be achieved with this configuration. This scheme may not be practical for a large system requiring radiation tolerant power sources.

ATLAS Micro Megas front-end board (mmfe8). The design has 8 VMM chips. From a common 12V input, three radiation tolerant FEAST DC-DC converter circuits provide power to the ASICs. A single FEAST supplies the digital rail (Vddd) to all 8 VMMs. For analog power the chips are divided into two sets of four VMMs. Each set has a FEAST supplying the analog power. The chips and rails within a chip are isolated with filter circuits. The general architecture is shown below.

Digital power

```
12V – FEAST – filter –|–  filter – 1V2_Vddd1  (chip 1)
                      |–  filter – 1V2_Vddd2  (chip 2)
                      |–  filter – 1V2_Vddd3  (chip 3)
                      |–  filter – 1V2_Vddd4  (chip 4)
                      |–  filter – 1V2_Vddd5  (chip 5)
                      |–  filter – 1V2_Vddd6  (chip 6)
                      |–  filter – 1V2_Vddd7  (chip 7)
                      |–  filter – 1V2_Vddd8  (chip 8)
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Analog power

```
12V – FEAST – filter –|–  filter –|– filter – 1V2_Vddp1    (chip 1)
                      |            |– filter – 1V2_Vdd1     (chip 1)
                      |            |– filter – 1V2_Vddad1   (chip 1)
                      |
                      |–  filter –|– filter – 1V2_Vddp2    (chip 2)
                      |            |– filter – 1V2_Vdd2     (chip 2)
                      |            |– filter – 1V2_Vddad2   (chip 2)
                      |
                      |–  filter –|– filter – 1V2_Vddp3    (chip 3)
                      |            |– filter – 1V2_Vdd3     (chip 3)
                      |            |– filter – 1V2_Vddad3   (chip 3)
                      |
                      |–  filter –|– filter – 1V2_Vddp4    (chip 4)
                                   |– filter – 1V2_Vdd4     (chip 4)
                                   |– filter – 1V2_Vddad4   (chip 4)
```

(similarly for chips 5 – 8 with a third FEAST)

ATLAS sTGC PAD front-end board (pFEB). The design has 3 VMM chips. From a common 10V input, two FEAST DC-DC circuits provide power to the VMM ASICs. The first FEAST supplies power to the digital rail (Vddd) and the ADC rail (Vddad) of the 3 VMMs. A second FEAST supplies the analog power rails (Vdd, Vddp) of the 3 VMMs. The general architecture is shown below.

Digital power

10V – FEAST – filter –|– 1V2_Vddd (chip 1)
|– 1V2_Vddad (chip 1)
|– 1V2_Vddd (chip 2)
|– 1V2_Vddad (chip 2)
|– 1V2_Vddd (chip 3)
|– 1V2_Vddad (chip 3)

Analog power

10V – FEAST – filter –|– 1V2_Vddp (chip 1)
|– 1V2_Vdd (chip 1)
|– 1V2_Vddp (chip 2)
|– 1V2_Vdd (chip 2)
|– 1V2_Vddp (chip 3)
|– 1V2_Vdd (chip 3)

Proposal for the SoLID prototype

We propose following the model of the ATLAS Micro Megas front-end card, isolating the analog and digital power rails using filters. The components shown below in red are placed on the power mezzanine card. The remaining filters are placed on the baseboard close to the VMM chips. The digital voltage 1V2D and analog voltage 1V2A generated on the power mezzanine card are carried to the base board through a pair of 2 blade micro power connectors (Samtec UMPT). Analog and digital grounds (AGND, DGND) may be separately carried to the baseboard on these connectors.

Digital power

```
                    1V2D
12V – FEAST – filter –|– filter – 1V2_Vddd1  (chip 1)
                      |– filter – 1V2_Vddd2  (chip 2)
```

Analog power

```
                    1V2A
12V – FEAST – filter –|– filter –|– filter – 1V2_Vddp1   (chip 1)
                      |          |– filter – 1V2_Vdd1    (chip 1)
                      |          |– filter – 1V2_Vddad1  (chip 1)
                      |
                      |– filter –|– filter – 1V2_Vddp2   (chip 2)
                                 |– filter – 1V2_Vdd2    (chip 2)
                                 |– filter – 1V2_Vddad2  (chip 2)
```

We propose relocating the VMM power micro connectors closer to the VMM chips as illustrated below.

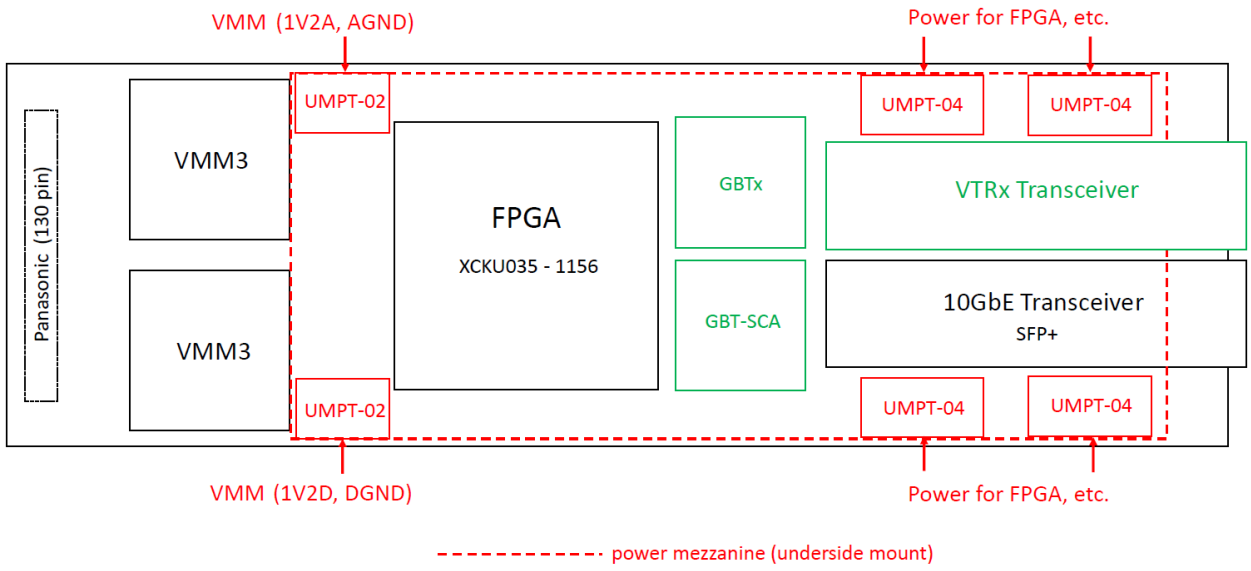

Figure 2. Power transfer points to VMM Prototype Card

Questions:

(1) Are there any issues in locating the power sources for the VMMs on a mezzanine card? No, as long as there is a very low impedance bringing analog supplies and grounds and sufficient and tailored (resonant frequencies) bypass capacitors

(2) Is locating the power entry points closer to the VMMs (as in Figure 2) a good idea? Yes, it looks fine as long as the FEAST is located far from that area

(3) Is the filtering scheme of the mmfe8 for the micro megas detector appropriate for our GEM detectors? Most probably yes

(4) Is it good design practice to place the filter circuits for VMM power as close to the VMM chips as possible? Yes

(5) The filters on the mmfe8 design that we are copying were optimized for the FEAST DC-DC power supply. If we instead use a low noise COTS power solution on the mezzanine card, is it O.K. to keep these same filters on the baseboard? Is there any downside to this? It is a good starting point, but it all depends on the performance of the COTS compared to the FEAST. Adjustments may be needed. Particular attention and specific rules should be dedicated to the layout and placement of the DC-DC components. If needed, please consult with George Iakovidis for the recommended rules.

(6) In terms of filtering, the approaches for the mmfe8 (micro megas) and the pFEB (sTGC) are very different. Do the VMMs for the sTGC detector operate at a lower gain than the VMMs for the micro megas detector? Is this why VMM power supply filtering is less important on the pFEB? Yes

(7) As I recall, the input and output grounds for the FEAST DC-DC circuit are the same. If we want to have separate analog and digital grounds (joined at point near the VMMs) this implies separate input supplies for the two FEASTS. Is it worth the effort to do this? (Both mmfe8 and pFEB use a single input supply.) No, but I am wondering why joining the analog and digital grounds near the VMMs rather than near the FEASTs, with maximum distance between each other along the two paths.

(8) Can the bulk of the FEAST filtering be done on the mezzanine card, with minimal isolation filters on the baseboard close to the VMMs? Yes

Follow up

It is appealing to do most of the filtering for the analog supply using tailored (resonant frequencies) bypass capacitors on the **mezzanine** card. This could be done once for the single analog voltage instead of duplicating the circuit 3 times on the main board. If this is done what would you suggest for baseboard filtering circuits that isolate the chips and the three analog voltages from each other?

*** **OR**, since the filtering system of the *mmfe8* board has been proven to be successful, is it safer to just copy it as is to our baseboard? Additional filtering can be done on the mezzanine card. We would like to avoid having to turn the baseboard again to correct for inadequate filtering.

The second option is much safer. It is critical that the impedance from supply to ground gets minimized in the frequency range of interest as seen from VMM. This means that the relevant capacitors should be placed as close as possible to VMM with plenty of vias where needed.