VMM prototype update – 11/11/21

- <u>VMM power mezzanine card</u>
 - PCB (6) shipped to JLab due 11/12/21
 - Quote for assembly due today. Fast track assembly using credit card (no wait for requisitions).

• FPGA power mezzanine card

- Replaced 'ultralow' noise regulator (LT3045) with 'low' noise regulator (LT3065). Layout requirements of LT3045 were demanding and difficult to satisfy in our application. LT3065 is more than adequate.
- Analyzed power dissipation in LTM4460 (4 x 4A supply). Efficiency is lower with +12V input. Small module package (15 x 9 x 5 mm) will dissipate ~6W at full load. To be able to handle future firmware changes we improved heat sinking capability of PCB (add copper on outside layers).
- Finalizing and reviewing these changes now
- Expect ready for PCB quote next week
- If cost is low enough we can fast track using credit card

VMM base board





VMM power mezzanine

FPGA power mezzanine

• VMM base board

- Base board to mezzanine connector update done
- Focus will shift to finishing this board after FPGA mezzanine PCB out for fabrication
- Measured two prototype GEMs at JLab and looked at design file of a UVA prototype GEM
- ALL have different distances between connector on GEM and edge of GEM frame
- To make prototype compatible with all prototype GEMs we moved GEM connector on base board to TOP side of board

Connector on BOTTOM side



- <u>About a final scheme for SoLID</u>
 - Most likely the final front-end cards for SoLID will support 4, 8, or more VMM chips
 - Makes sense point of load power system can be scaled up efficiently for more VMMs and more (or bigger) FPGAs
 - How do we connect the GEM with a front-end card that supports many more channels?
 - What we learned about tight connector alignment tolerances between base and mezzanine boards joined with <u>multiple</u> connectors **also applies to the GEM front end card interface**
 - To avoid difficulties we should join the GEM and front-end card with a <u>single</u> high-pin count connector if possible