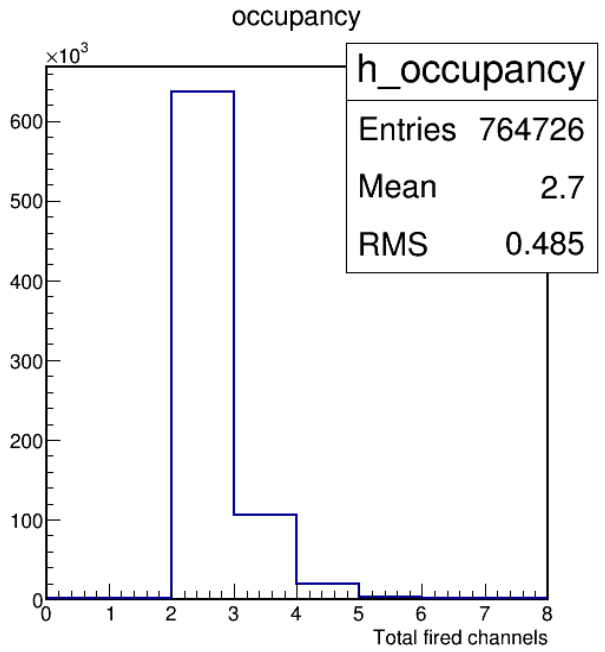
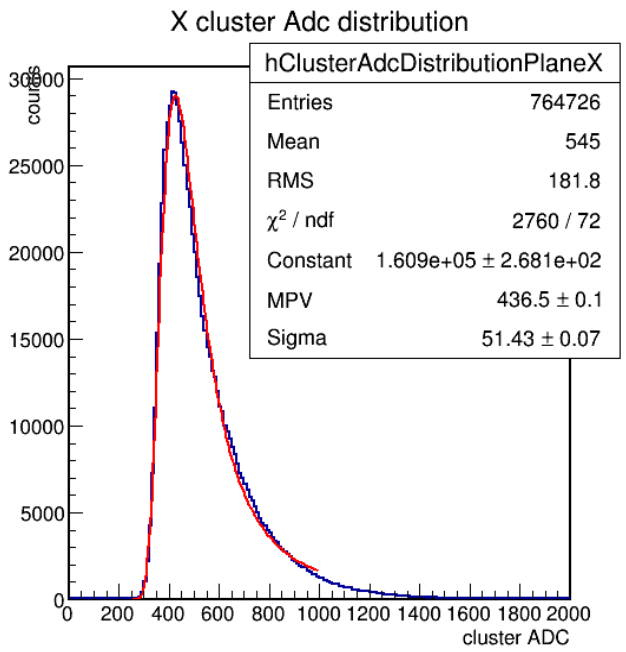
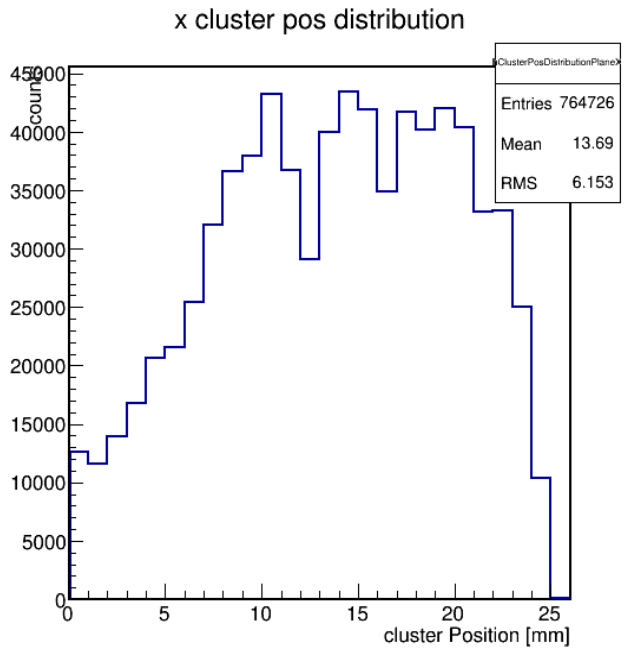
Cosmic and Sr-90

- Cosmic run using scintillator trigger (external with latency set)
- Sr-90 run using internal trigger, send 1-ms period test pulse trigger to VMM
- Cluster size: 2 – 5, to cut away a few hot channels in VMM chip

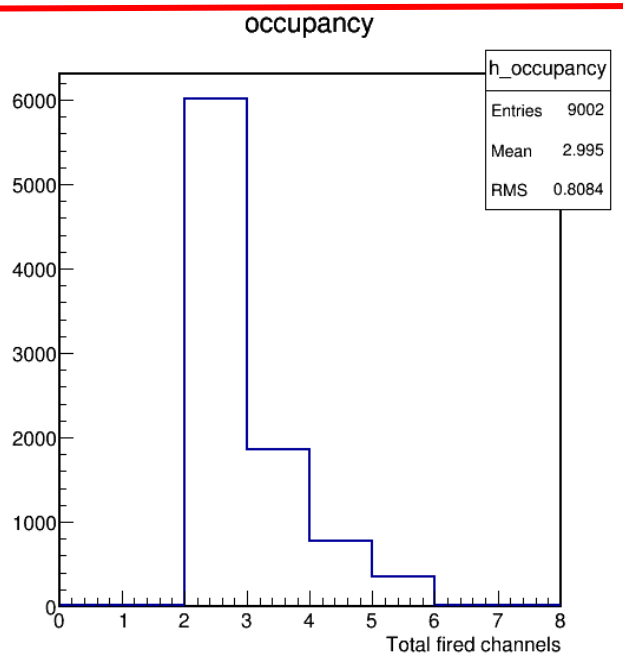
Sr90

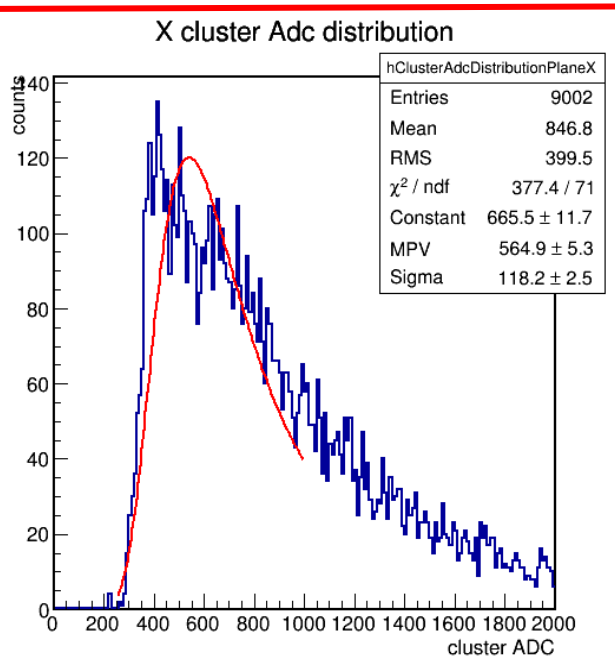

occupancy
h_occupancy
Entries 764726
Mean 2.7
RMS 0.485
Total fired channels

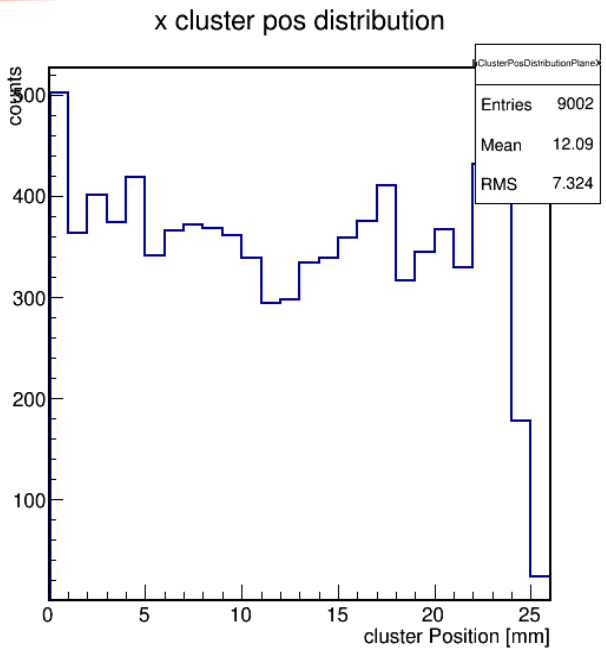

X cluster Adc distribution
hClusterAdcDistributionPlaneX
Entries 764726
Mean 545
RMS 181.8
χ² / ndf 2760 / 72
Constant 1.609e+05 ± 2.681e+02
MPV 436.5 ± 0.1
Sigma 51.43 ± 0.07
counts
cluster ADC


x cluster pos distribution
Entries 764726
Mean 13.69
RMS 6.153
counts
cluster Position [mm]

Cosmic


occupancy
h_occupancy
Entries 9002
Mean 2.995
RMS 0.8084
Total fired channels


X cluster Adc distribution
hClusterAdcDistributionPlaneX
Entries 9002
Mean 846.8
RMS 399.5
χ² / ndf 377.4 / 71
Constant 665.5 ± 11.7
MPV 564.9 ± 5.3
Sigma 118.2 ± 2.5
counts
cluster ADC

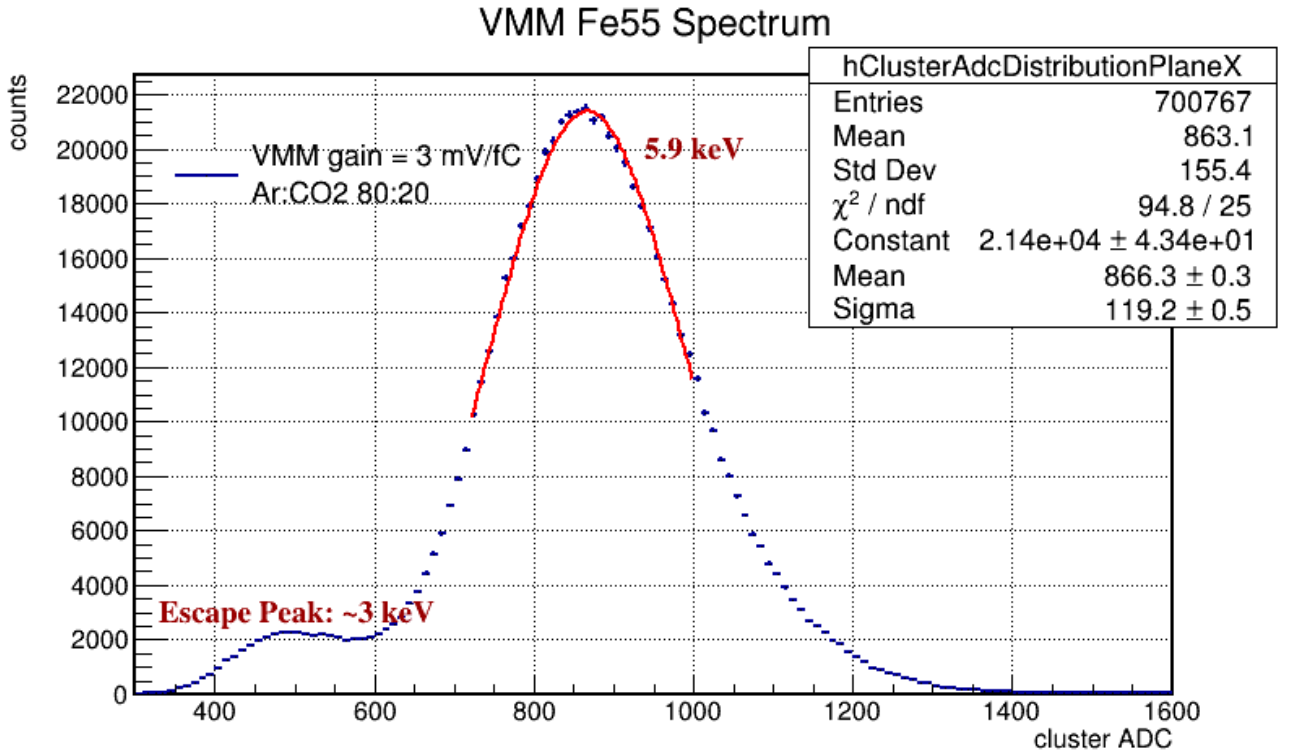

x cluster pos distribution
Entries 9002
Mean 12.09
RMS 7.324
counts
cluster Position [mm]

Detector Gain from Fe55 source

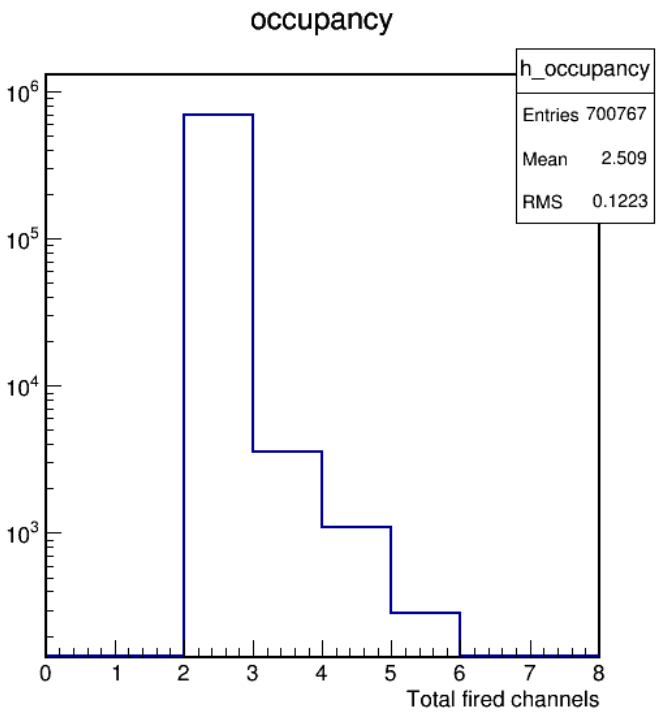
- Fe55 X-ray Source
- 5.9 keV main peak, 2.9 keV Argon escape peak
- GEM HV 3900 V
- Gas ratio Argon:CO_2 = 80:20
- W: 25 eV (Argon), 34 eV (CO_2)
- Primary Ionization (main peak): 5.9 keV / (0.8 * 25 + 0.2*34) ~ 220

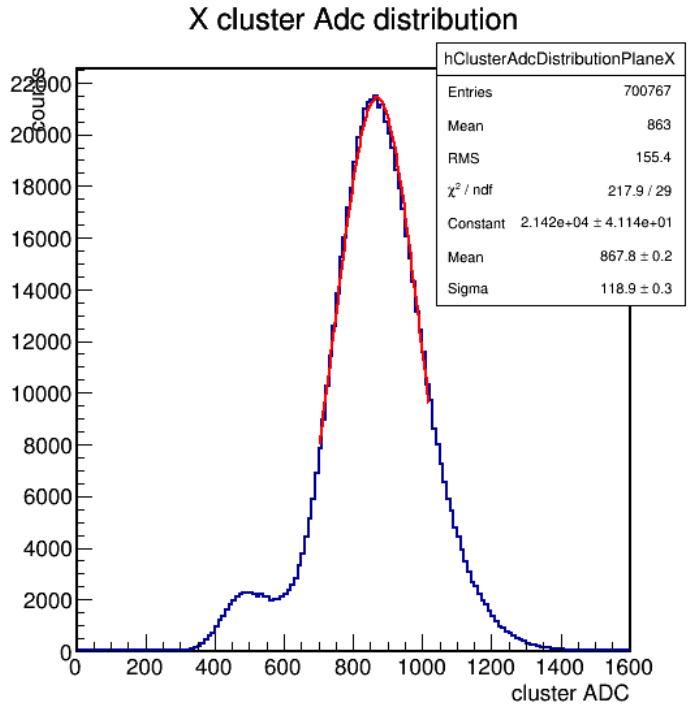
Fe55 spectrum

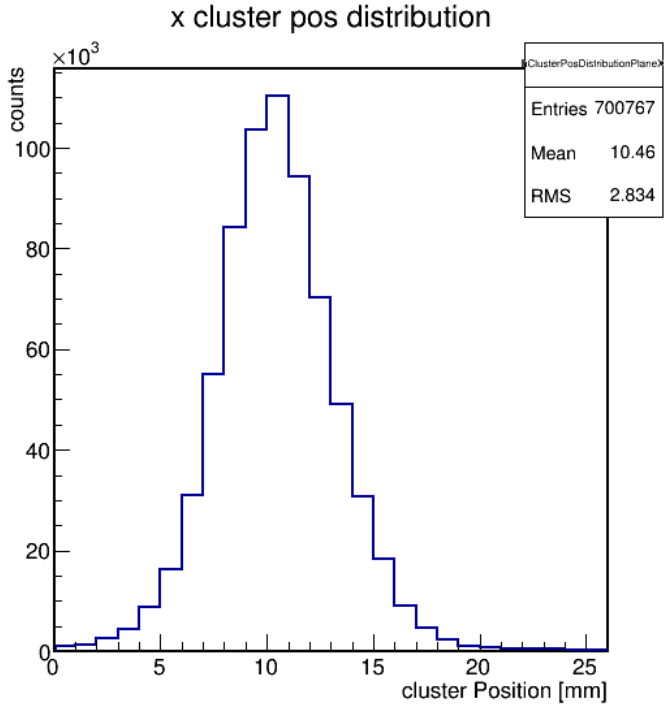
- VMM gain = 3 mV/fC
- 1 fC = 6421.5 electrons
- Main peak ADC = 866
- Conversion factor (10 bit ADC, resolution 1 mV): 1.024
- The main peak is around 845.7 mV, ~ 281.9 fC
- Main peak = 1810227.5 electrons
- Detector gain: 8228.3
- Results could be improved after VMM chip calibration



Fe55


occupancy
h_occupancy
Entries 700767
Mean 2.509
RMS 0.1223
Total fired channels


X cluster Adc distribution
hClusterAdcDistributionPlaneX
Entries 700767
Mean 863
RMS 155.4
χ² / ndf 217.9 / 29
Constant 2.142e+04 ± 4.114e+01
Mean 867.8 ± 0.2
Sigma 118.9 ± 0.3
counts
cluster ADC


x cluster pos distribution
×10³
Entries 700767
Mean 10.46
RMS 2.834
counts
cluster Position [mm]

VMM calibration

1. DAC calibration (including pulser DAC and global threshold DAC)
2. Baseline and Noise measurement
3. Channel threshold trimming
4. Signal amplitude gain and pedestal
5. Timing calibration

DAC calibration

- DAC (pulser and global threshold) can be routed to the VMM MO output
- MO output can be digitized by the xADC (in an external FPGA)
- xADC is 12-bit, reference voltage 1 V

- Methods: try a series of different DAC values, measure it using xADC, get the slope and intercept of the mV – DAC relationship
- The slope and the intercept can be used to convert the DAC value to voltage

Channel baseline and noise

- Measured by the xADC
- Goal: measure the ambient level for each channel when no signal is applied

- Methods: measure each channels' output using xADC
- Get the average and sigma from the measurement
- Average = baseline, sigma = noise
- Both on and off the detector need it
- When setting the threshold: threshold = baseline + 3 * sigma

Channel threshold trimming

- Threshold has channel-to-channel variation
- To make all channels have the same response to input signals, need to equalize the threshold
- On top of the global threshold, each channels has its own 5-bit trimming-DAC
- Channel's threshold can be fine-adjusted using this 5-bit DAC, in 32 steps, each step ~ 1 mV

- Methods: using xADC measure the threshold for each channel (measure all 32 steps)
- When done, for all channels, choose one common value that closest to the global threshold
- Then each channel's corresponding step (5-bit ADC value) constructs the table needed to equalize the threshold
- This table is independent of global threshold, one can then adjust the global threshold to affect all channels coherently

Signal amplitude gain and pedestal

- AKA PDO calibration
- For a given signal, channel response is different (fluctuate around the global gain setting)
- Two calibration methods: 1) using DAC pulser; 2) using neighbor logic
- DAC pulser method:
  - First finish the DAC calibration
  - Measure PDO with a series of different DAC pulser
  - Get the slope and y-intercept between PDO – DAC for each channel
  - Slope is the channel gain, y-intercept is the channel pedestal
  - Y-intercept must be subtracted when doing the physics analysis
- Neighbor logic method
  - Enable neighbor logic means when a strip was fired, its neighboring strips will also be recorded, no matter neighboring strips are fired or not
  - We can directly measure the pedestal of each channel, by giving its neighbor strip a test pulse
  - Only pedestal, cannot do gain measurement

Timing measurement calibration

- Timing-at-peak, timing-at-threshold
  - Timing-at-peak, TAC starts to ramp when PDO detects signal peak
  - Timing-at-threshold, TAC starts to ramp when signal crosses threshold
- Configurable TAC ramp time (60ns, 100ns, 350ns…)
- Normal mode, fix-window mode
  - Normal mode: TAC halts at the next BC clock falling edge
  - Fix-window mode: BC clock is paused for a fixed time/latency, after that BC clock is re-initiated, and TAC also halts at the first new BC clock falling edge
- The fixed-latency mode calibration
  - allows a fine timing measurement calibration, by changing the fixed latency, and then measure the TDO readout per channel
  - A TDO – Latency (time) plot gives the slope and y-intercept
  - The slope and y-intercept are used to extract time from TDO
- Normal mode calibration
  - By skewing the test pulse and the BC clock
  - The bigger the time difference between TP and BC, the shorter the TAC integration duration
  - Similar procedure to extract the slope and y-intercept
- Timing-at-threshold is often affected by timewalk issue, needs correction