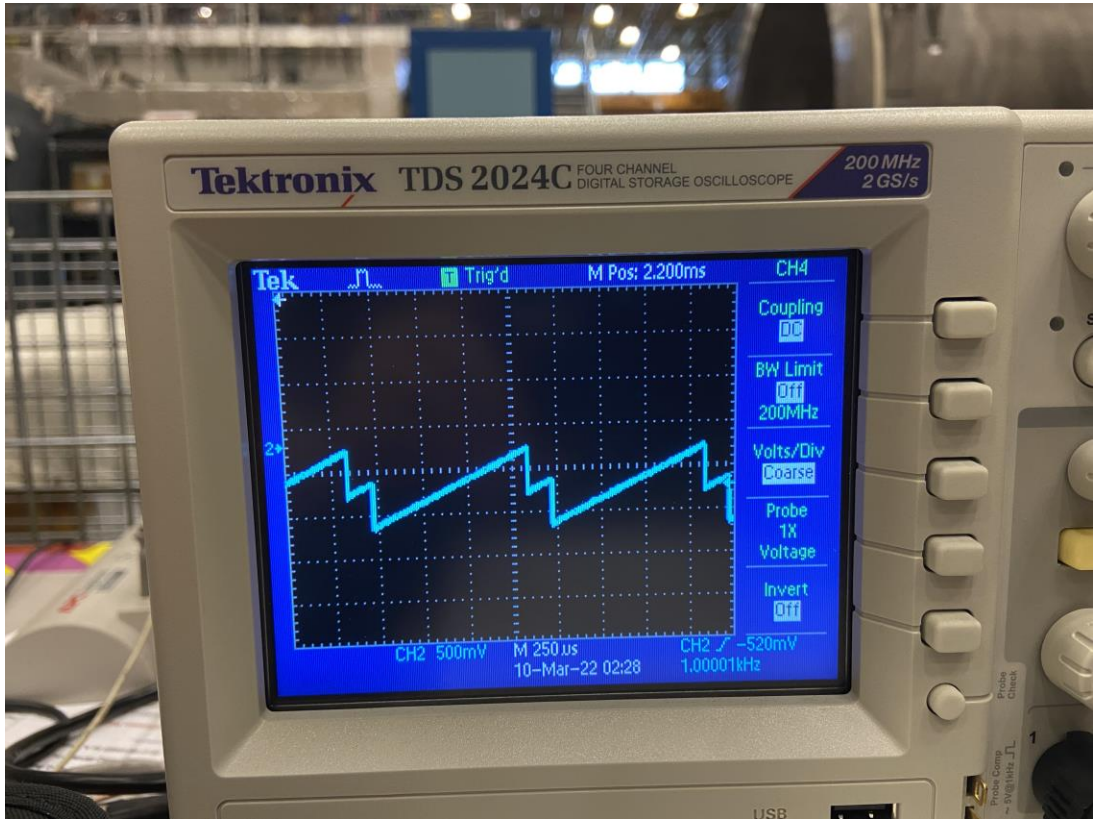
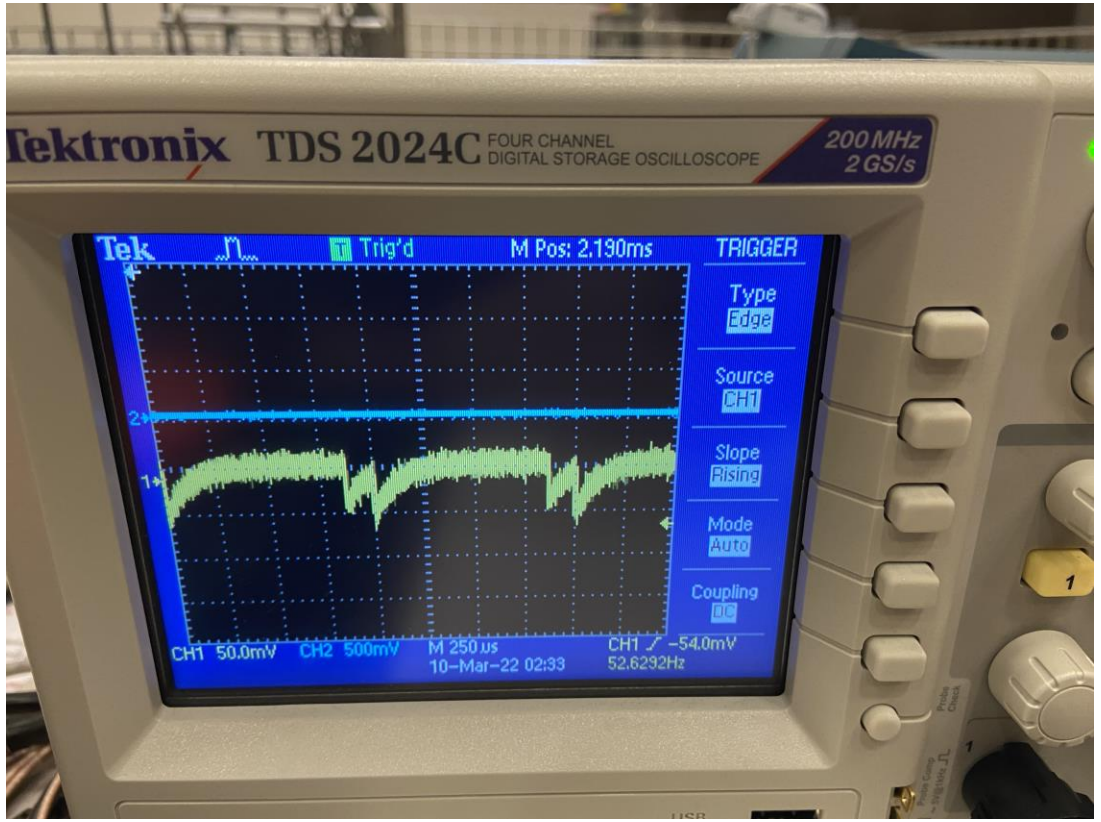
# Pileup signal – This method seems works




Pulser Signal

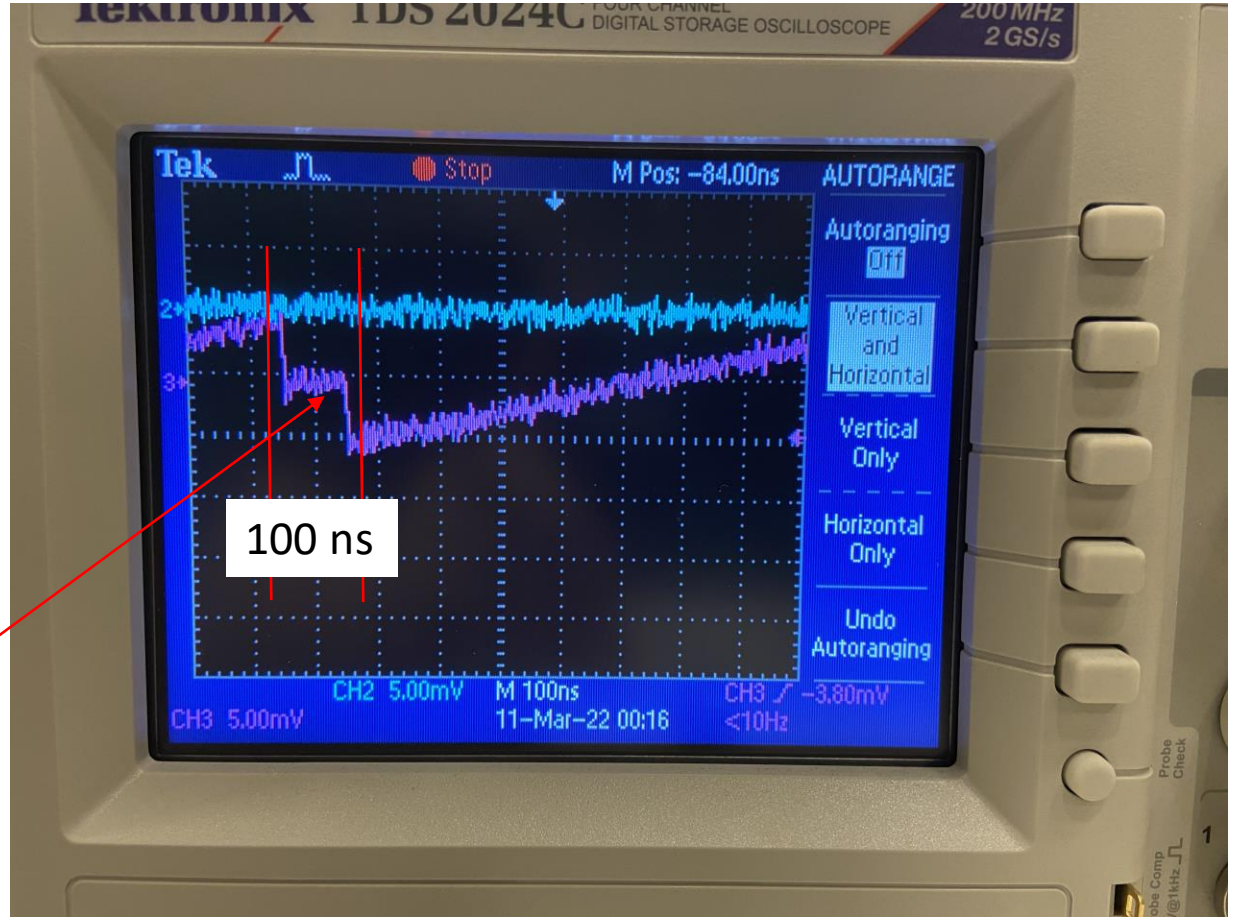



Pileup signal to VMM chip

# Pileup signal – Something not perfect

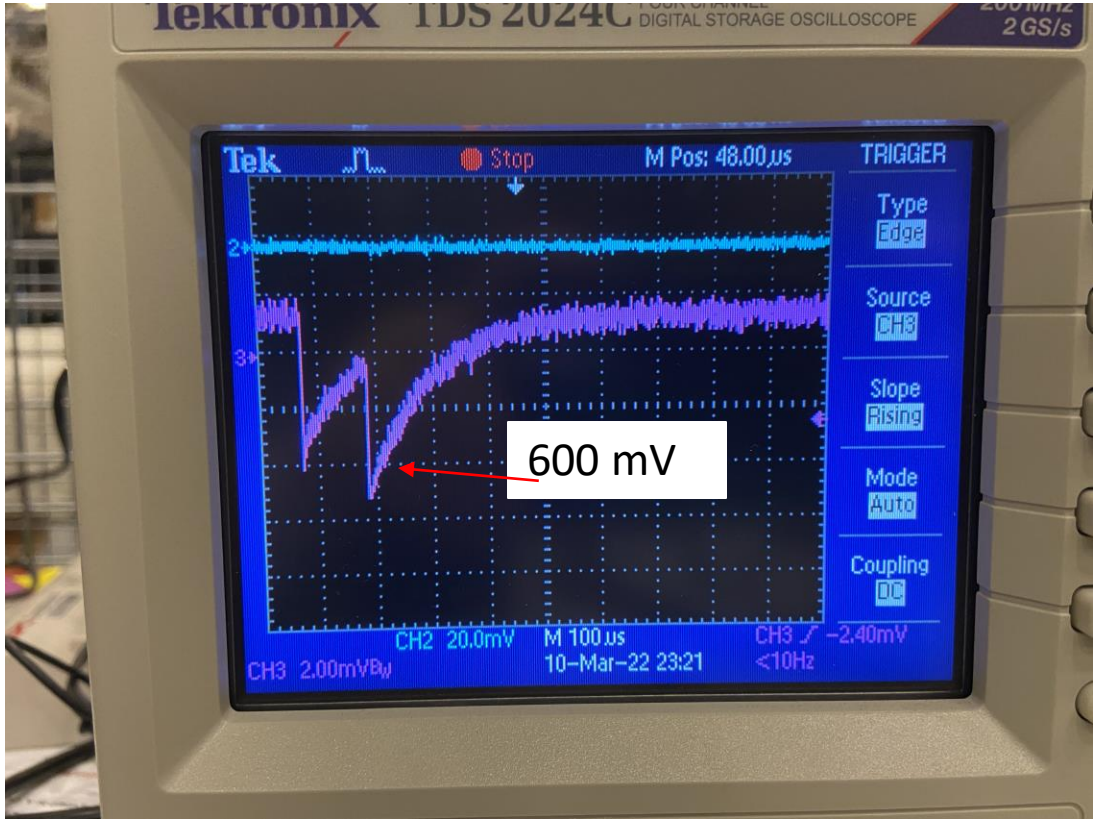
- This is the capacitor network output
- To get pileup signals, I need two peaks separation < 200 ns
- Otherwise the VMM chip can distinguish the two pulses
- But when the separation between two peaks is small, I get almost a flat line, not sure this can be treated as a pileup signal when VMM chip tries to find a "peak"

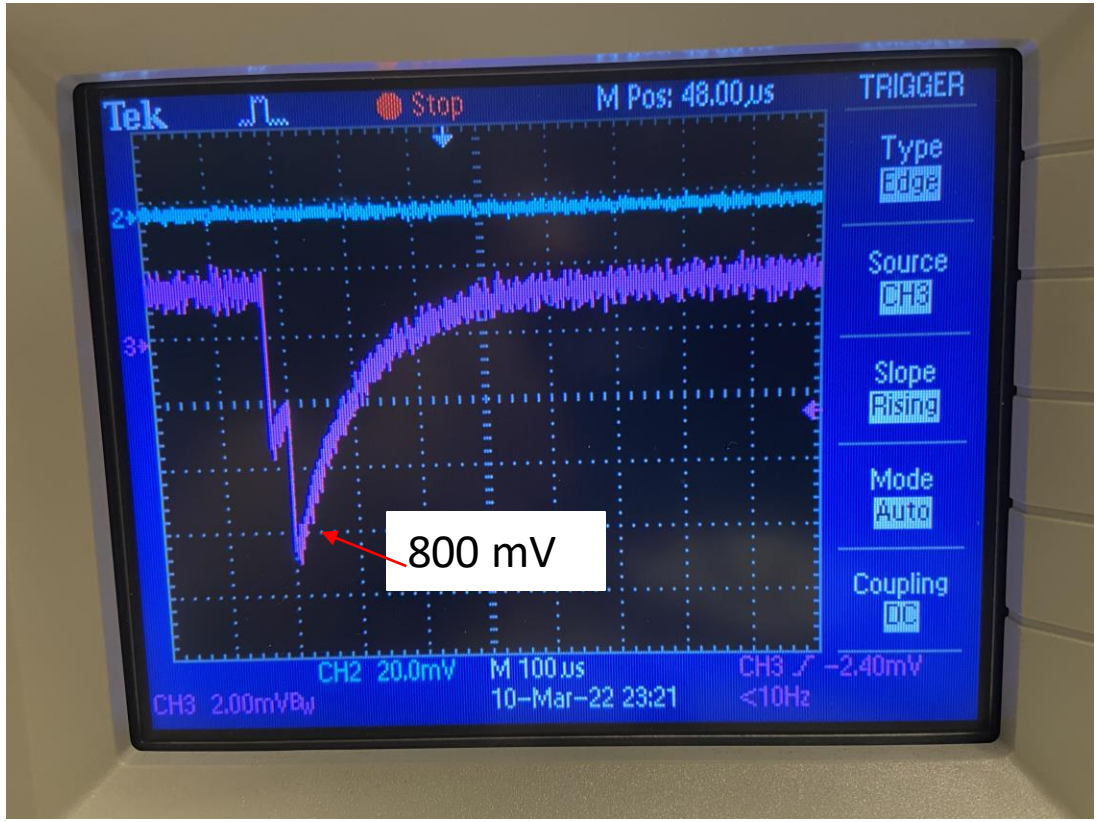
**This is a bit flat**



# Backup Slides

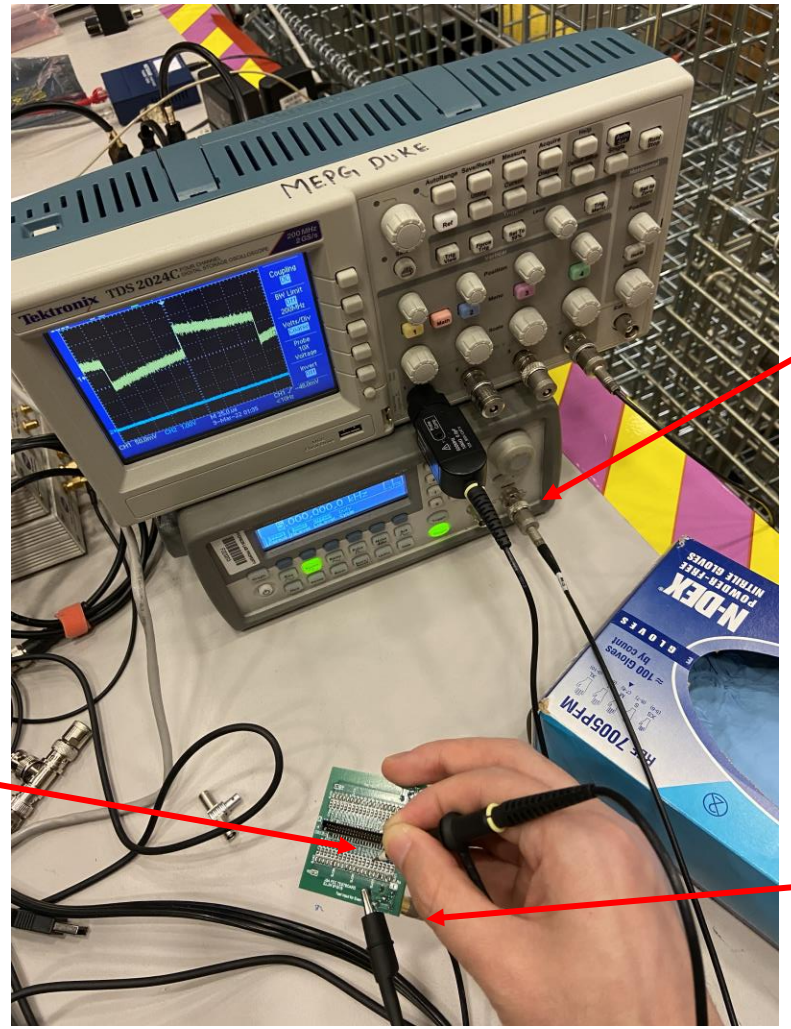
# Signal amplitude increased when closer



# Pileup signal generator

- Pulse signal from generator
- Pulser signal to the VMM pulsing board
- Adjust pulser setting to generate pulse signals




Generator Pulser

Signal to VMM input

Pulsing board