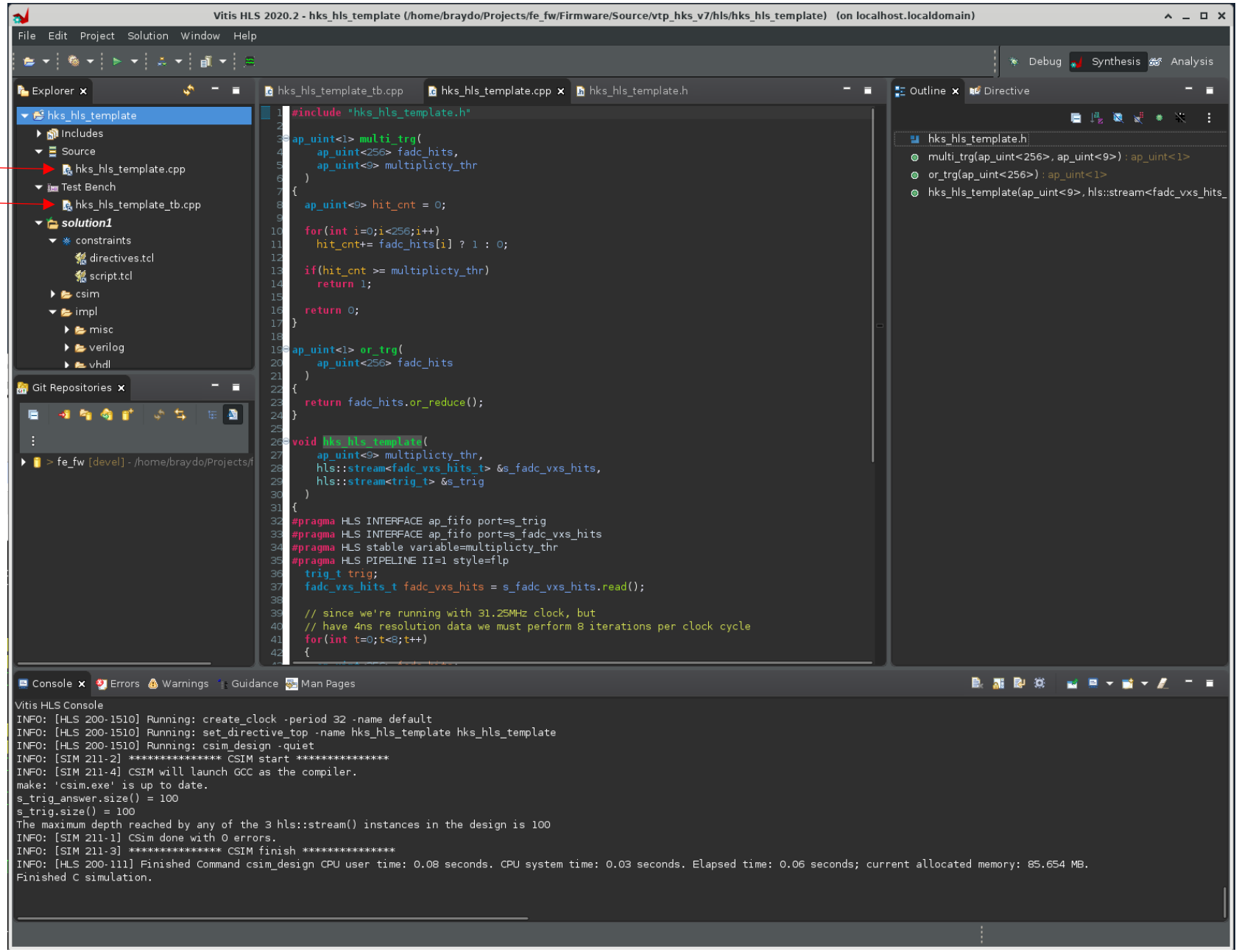
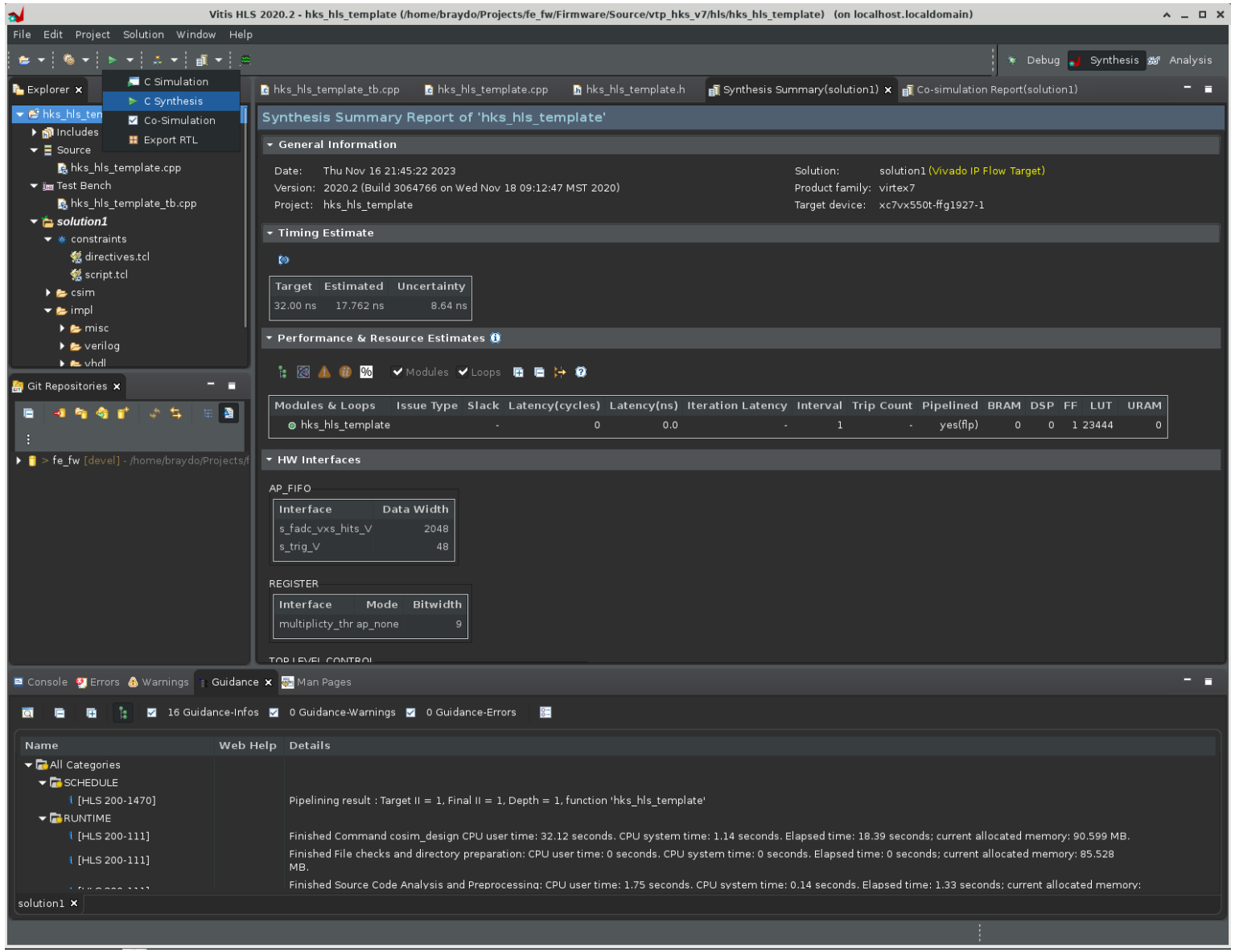
Synthesis C++ target

C++ testbench



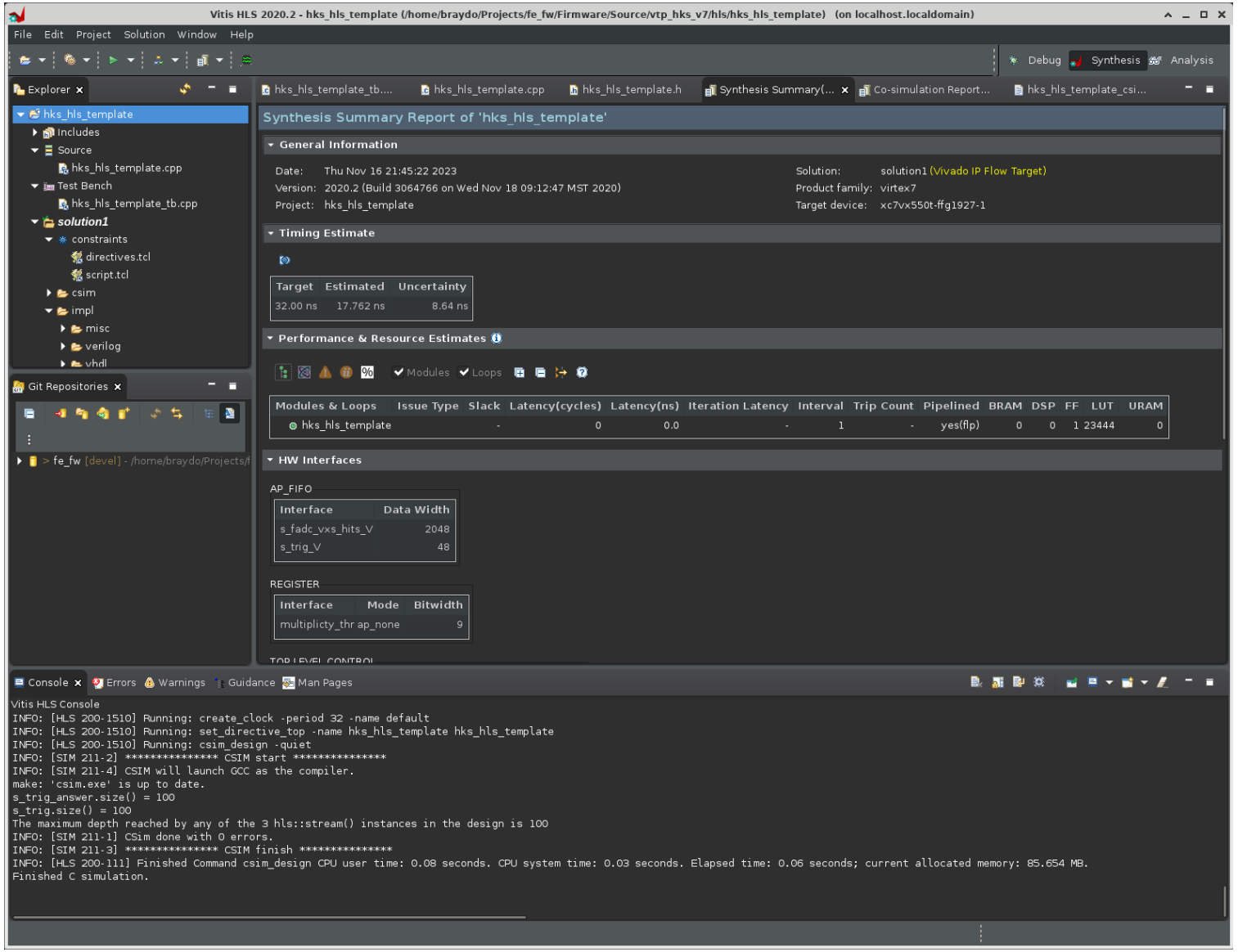
Main functions to run:

1) C Synthesis
2) C Simulation
3) Co-Simulation



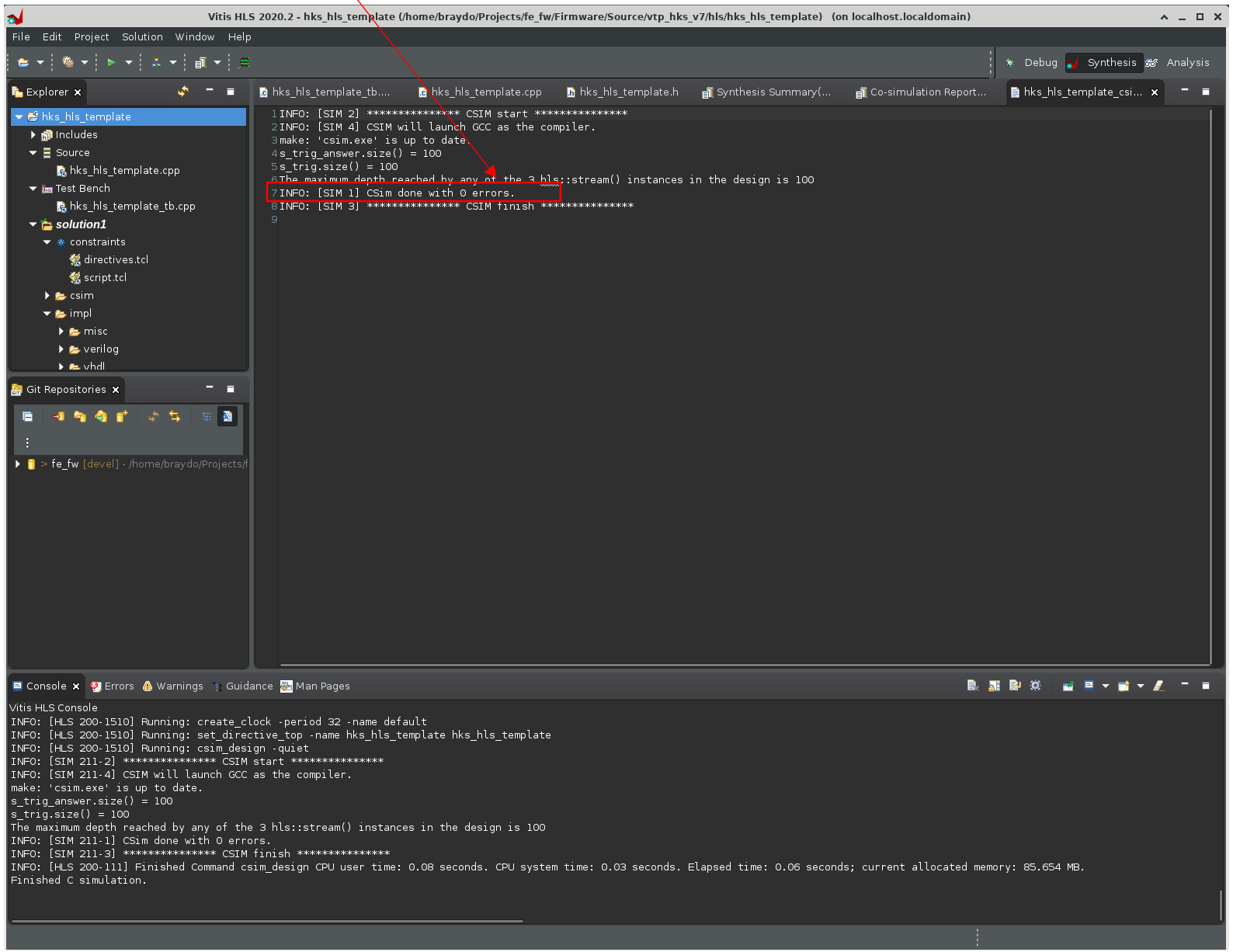
## C-Synthesis – synthesizes VHDL/Verilog source files from C/C++ code

C-Synthesis result: latency(cycles) should be small (<30), Interval=1, BRAM<200, DSP<200, FF<200k, LUT<200k, URAM=0



# C-Simulation – Verify C/C++ code works by feeding it data and checking result

C-Simulation result: no errors (based on hks_hls_template_tb.cpp main() returning value of 0



# Co-Simulation – Simulates HDL solution and verifies it with C++ testbench input/output check. Waveform can be viewed as shown to see digital waveforms and inspect inside the HLS VHDL/Verilog solution if needed