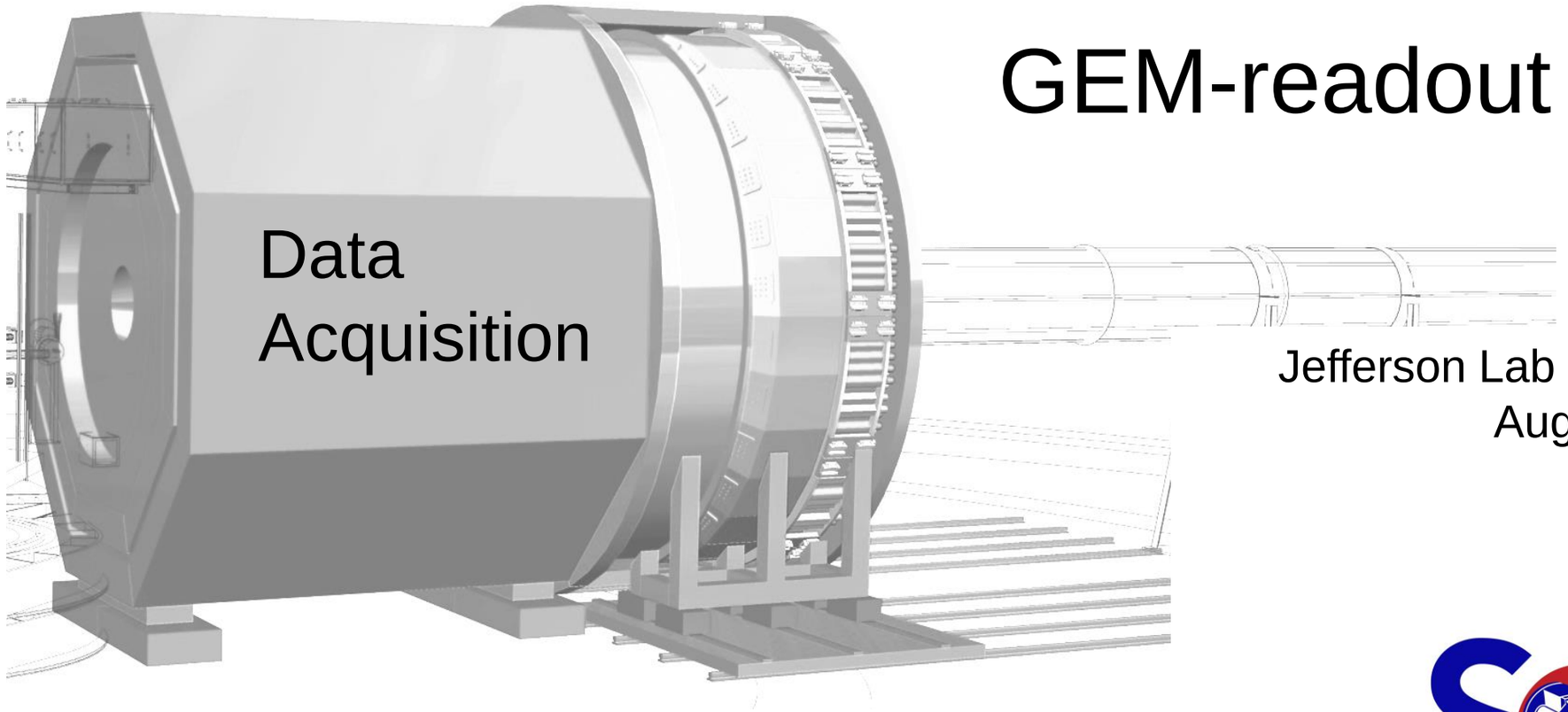


GEM-readout development

Data Acquisition

Jefferson Lab SoLID Pre-R&D Review
August 7th, 2020

Ed Jastrzembski

Data acquisition working group
JLab FE-DAQ Group

Outline

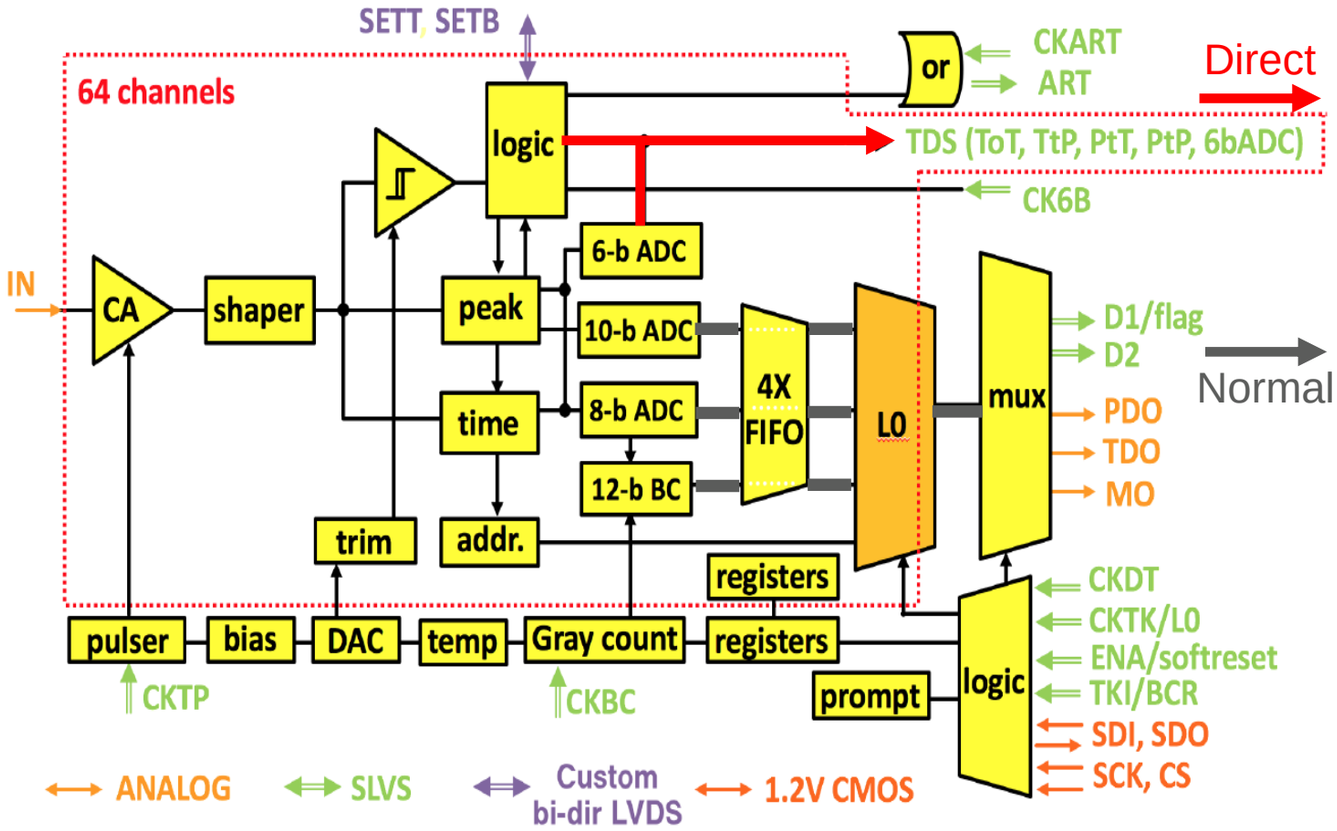
- SoLID preRD goals for VMM3
- VMM3 overview and use in the ATLAS experiment
- Concept for VMM3 readout
- VMM3 prototype board
- Options for VMM3 readout card
- VMM3 evaluation boards
- APV25 readout of GEMs in SoLID
- Appendix (rate calculation)

SoLID preRD goals for VMM3

- Flux of 1 MHz/cm2 results in rates of several MHz for some GEM strips
- Need to minimize front-end dead time and be able to read out high data volume resulting from trigger rates beyond 100 KHz
- The VMM3 chip offers a fast 6-bit A/D conversion of the peak amplitude, resulting in a dead time of ~50 ns
- Need to implement VMM3 prototype to test if this fast direct readout mode produces data with quality sufficient for tracking in high backgrounds
- If it does, identify possible final readout solution of VMM3 for SoLID

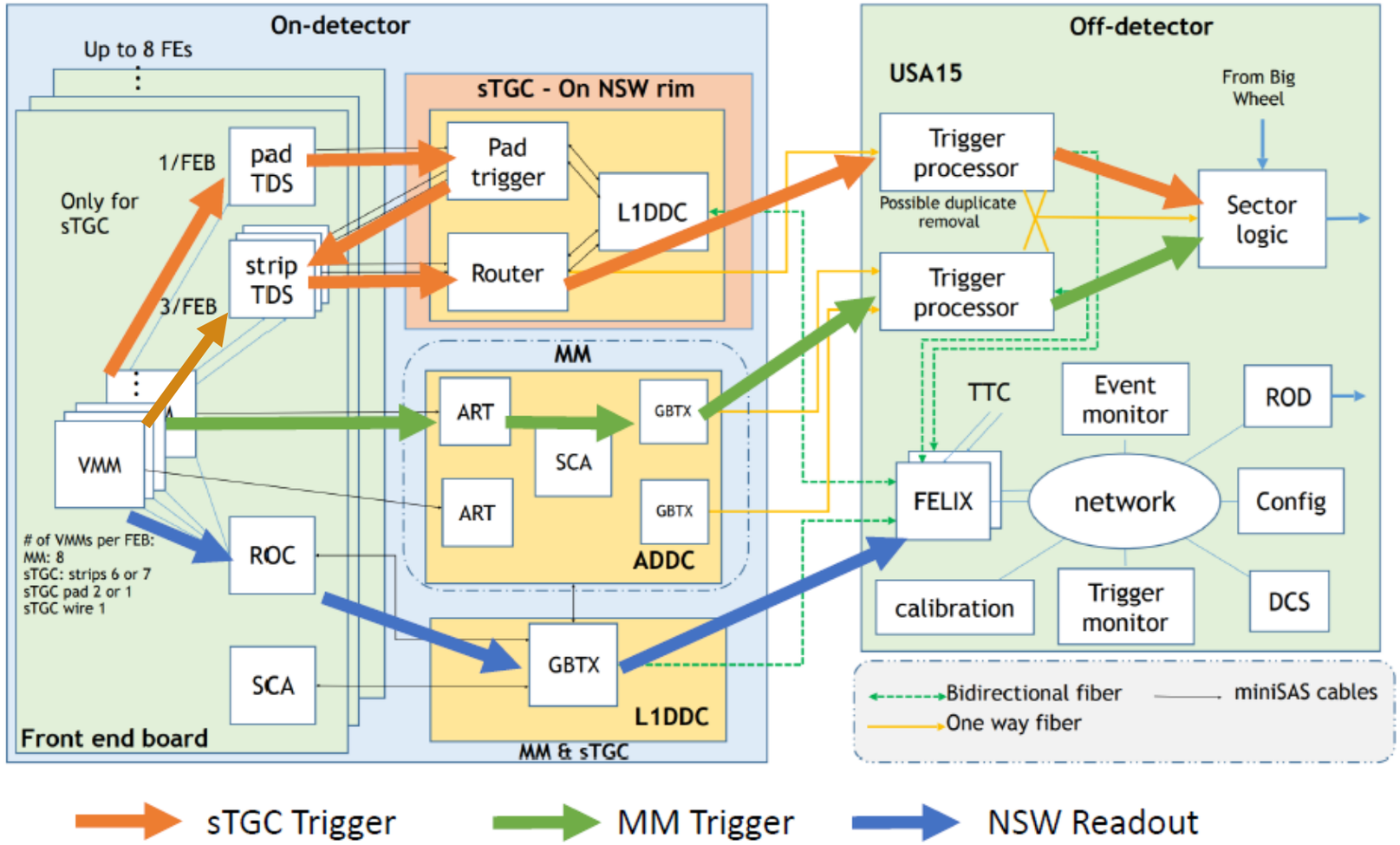
VMM3 chip

VMM3 block diagram



- ASIC for ATLAS New Small Wheel
- Radiation hard similar to APV25 : > 100 Mrad
- 64 channels
- Low noise over wide range of input capacitance (<1 pF to ~1 nF)
- Shaping times : 25 ns, 50 ns, 100 ns, 200 ns
- Pulse amplitude proportional to charge at input
- Gains : 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC
- **6 bit ADC (25 ns conversion)** and **10 bit ADC (250 ns conversion)**, 8 bits TDC (1 ns resolution), 12 bits Beam Crossing time stamp
- 4 MHz of rate per channel thanks to multilevel FIFO
- Continuous or triggered readout on normal data path
- Latency up to 16 μs in triggered mode
- **Fast direct outputs (64 channels) for ATLAS trigger (6b ADC, ToT)**
- Normal data link up to 320 Mb/s

ATLAS New Small Wheel Trigger and Readout



(VMM direct outputs)

Radiation tolerant ASICs:

- VMM (amplifier, shaper, discriminator)
- Read Out Controller (ROC)
- Trigger Data Serialiser (TDS)
- Address Real Time (ART)
- Slow Control Adapter (SCA)
- GigaBit Transceiver (GBTX)

PCBs:

pFEB/sFEB(sTGC pad/strip front-end board)

MMFE8(Micromegas front-end board)

L1DDC(Level-1 Data Drive Card)

Pad Trigger

Router

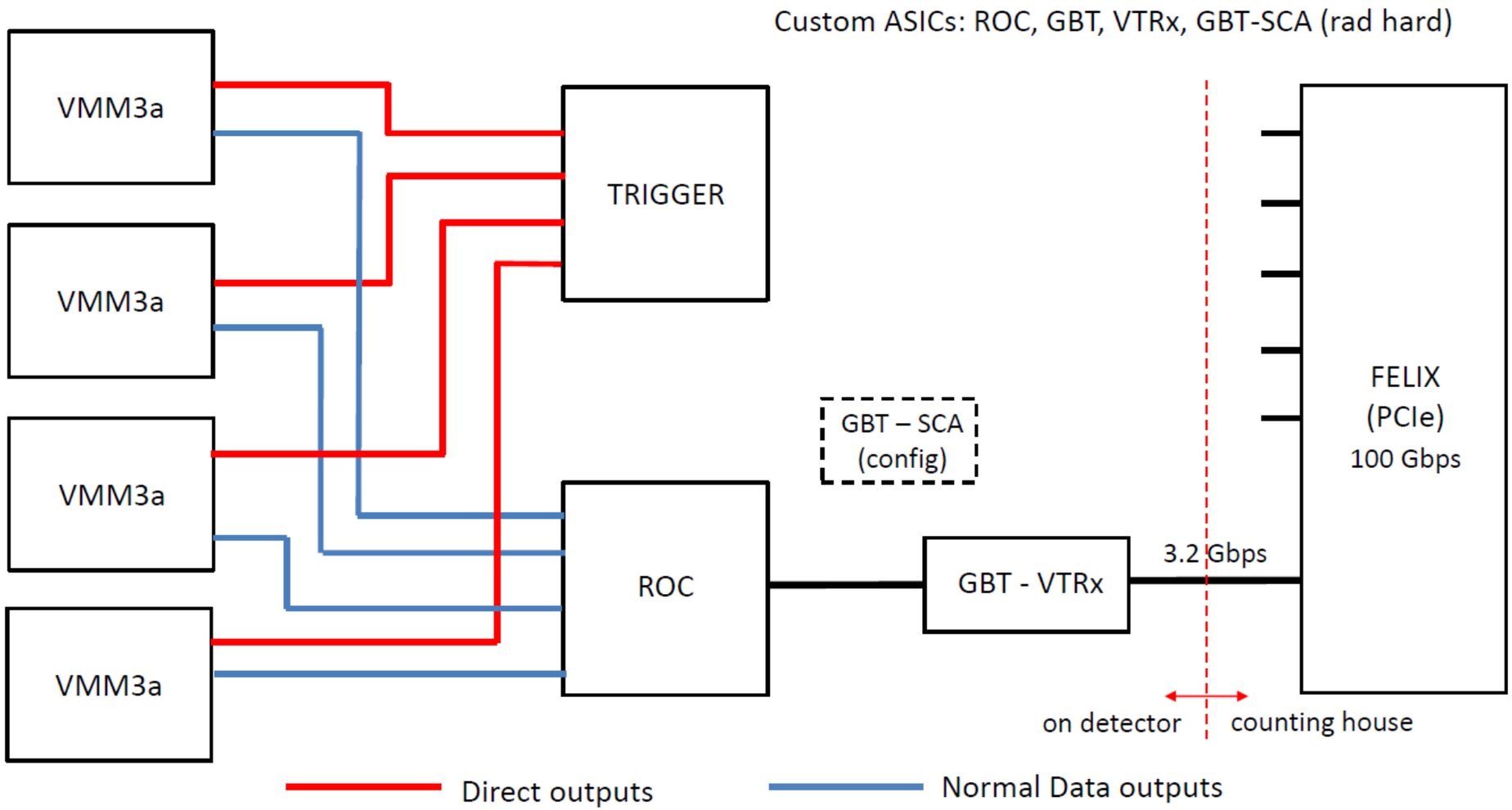
ADDC

FELIX(Front-End LInk eXchange)

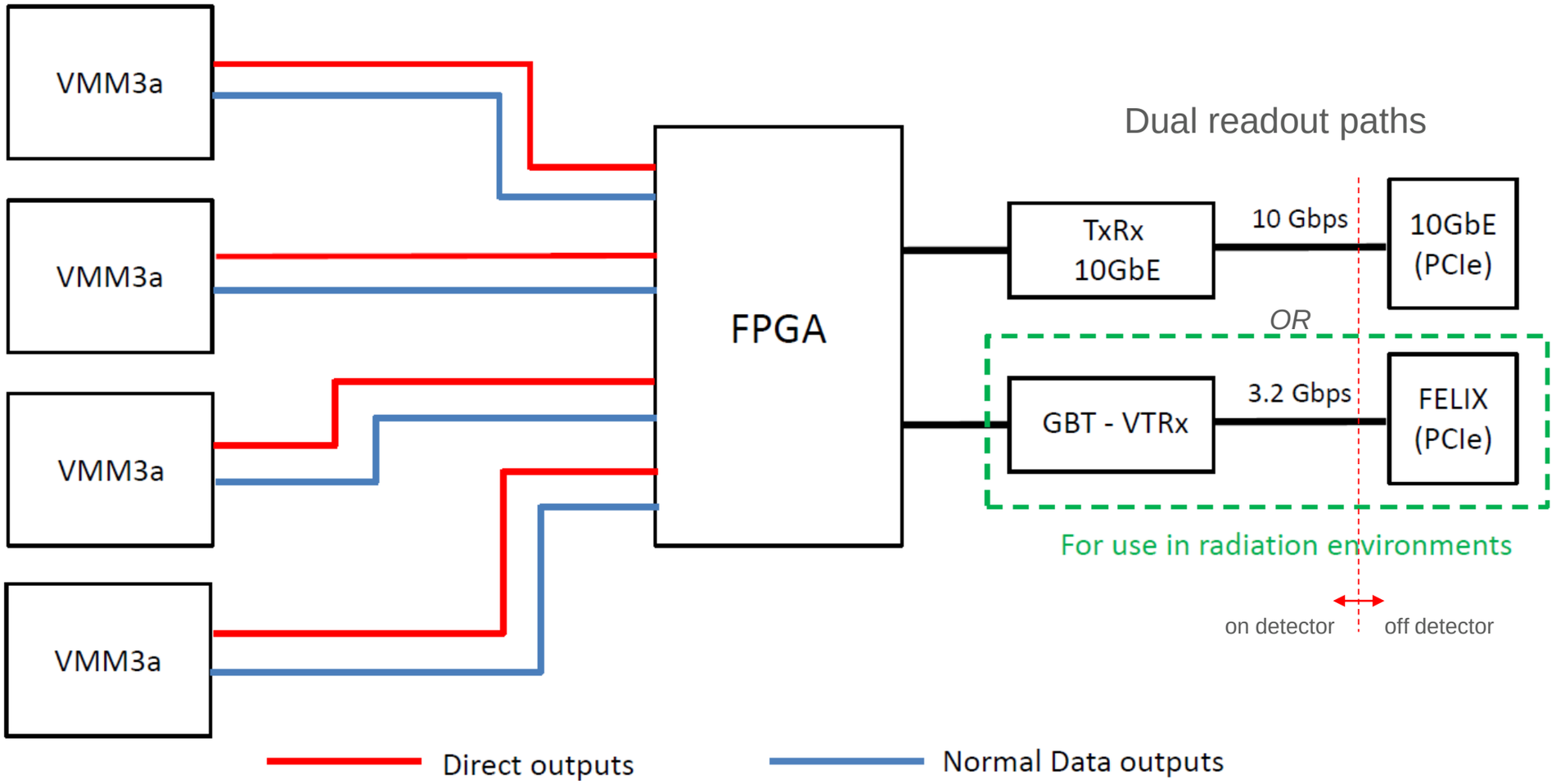
Trigger Processor

7

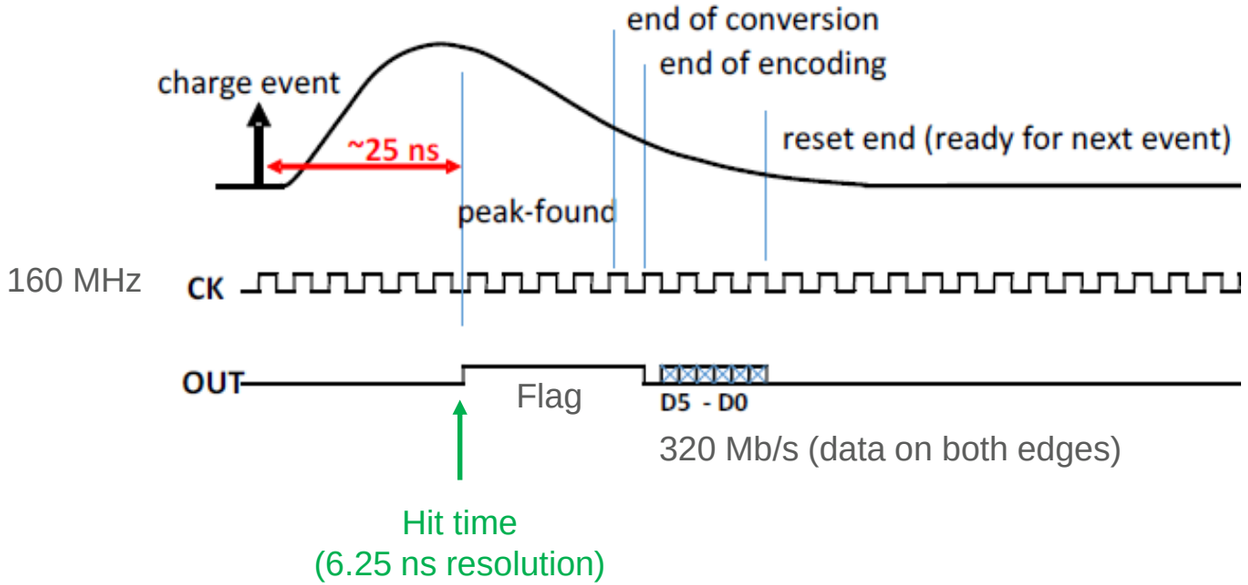
ATLAS New Small Wheel Trigger and Readout (simplified)



Concept for VMM3 readout

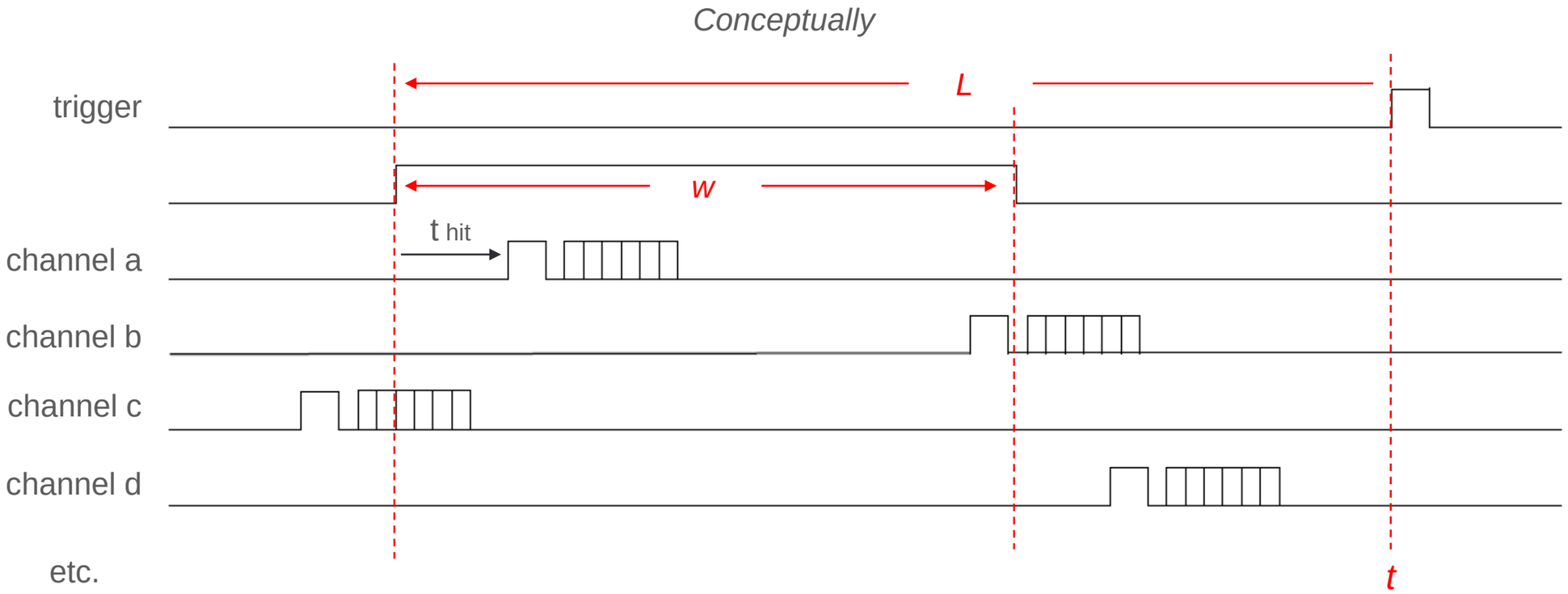


6-bit Direct output data format



FPGA function

- Direct output data from the VMM3 chips is continuously written into a circular buffer in the FPGA.
- Let *L* be the trigger latency (*L* < 8 μs) and *w* be the data capture window size (*w* < 0.8 μs)
- Upon receipt of a trigger at time *t*, data corresponding to the time period [*t* – *L*, *t* – *L* + *w*] is captured and formatted for transmission off the chip



FPGA function

- If rising edge of flag for direct output data is within capture window, serial data that follows is accepted
- In practice, de-serialize 6-bit data at input – trade increased width of buffer for slower clock rate (160 MHz)
- Time of hit is recorded as time relative to window start (7 bits)
- Include bits for channel number (8 bits), number of hits for channel (5 bits), status bits (4)
- Header with trigger time stamp (32 bits), trigger number (16 bits)
- **(See Appendix for details)**
- Data transmitted to GBT chip on **10** serial e-links (**320 Mb/s** each)
- (High-speed serialization by GBT (3.2 Gb/s) – fiber transmission (VTRx) to FELIX PCIe readout card)

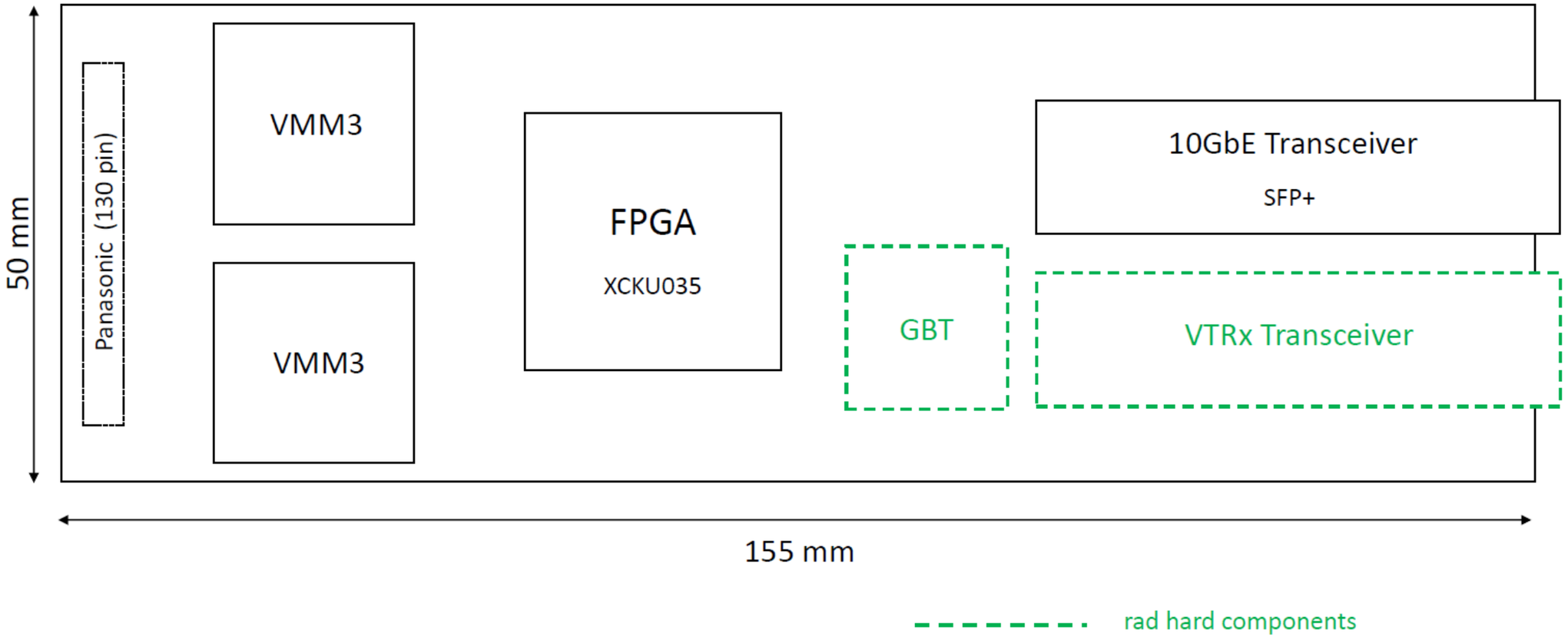
Data rates

- Let *r* be the hit rate for a channel (MHz), and *w* be the data capture window size (μs)
- Assume that all 256 channels (**4 VMM3**) have the same hit rate *r*, and that *w* < 0.8 μs
- Using the bit assignments described in the **Appendix**, we can find the relationship of *r*, *w*, and the maximum trigger rate such that the GBT link is completely saturated (3.2 Gb/s):
- *Trigger rate* (max) = (3200 Mb/s) / (4912 + *w***r**3328 b)

r (MHz)	*w* (μs)	*r***w*	*Trigger rate* (KHz)
1	0.5	0.5	486
2	0.5	1.0	388
4	0.5	2.0	276
8	0.5	4.0	175

VMM3 Prototype Board

For simplicity we use 2 VMM3 chips



VMM3 Prototype Board

- Xilinx Kintex UltraScale FPGA (KCKU035)
  - Compatible with receiving low level **SLVS** signals from VMM3
  - Good immunity against radiation induced ‘latch-up’
  - Detect and correct radiation induced SEUs (Single Event Upsets) in configuration memory with Xilinx IP
  - Use redundant design techniques (TMR –Triple Modular Redundancy) to mitigate against SEUs in user logic
  - Footprint compatible with KCKU040 FPGA with 20% more internal resources
- Support components also sensitive to the effects of radiation
  - Power components (linear regulators, DC-DC converters)
  - Commercial grade (COTS) power components can fail – no mitigation techniques available
  - Many radiation measurements on COTS components have been made (ATLAS database, space research); show large lot-to-lot variations
  - Space grade components are too expensive and hard to get
  - Can use rad hard CERN FEAST DC-DC converter modules for all power
  - 5 voltages required: VMM: 1.2V analog, **1.2V** digital; FPGA: 0.95V, **1.2V**, 1.8V, 2.5V

CERN FEAST DC-DC Converter Module

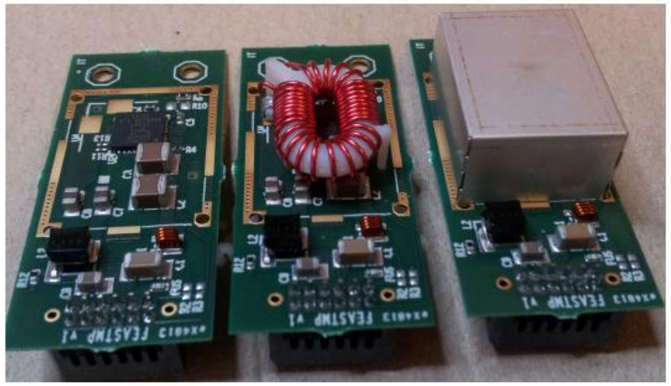


Figure 1: View of the FEASTMP module fully assembled (right), with shield removed (center) and with main inductor removed (left).

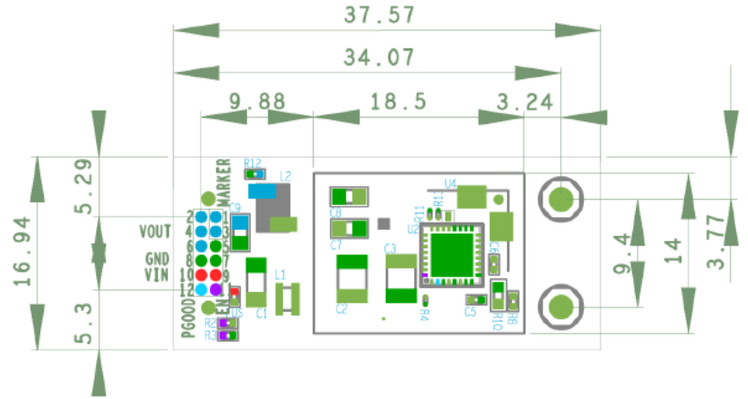


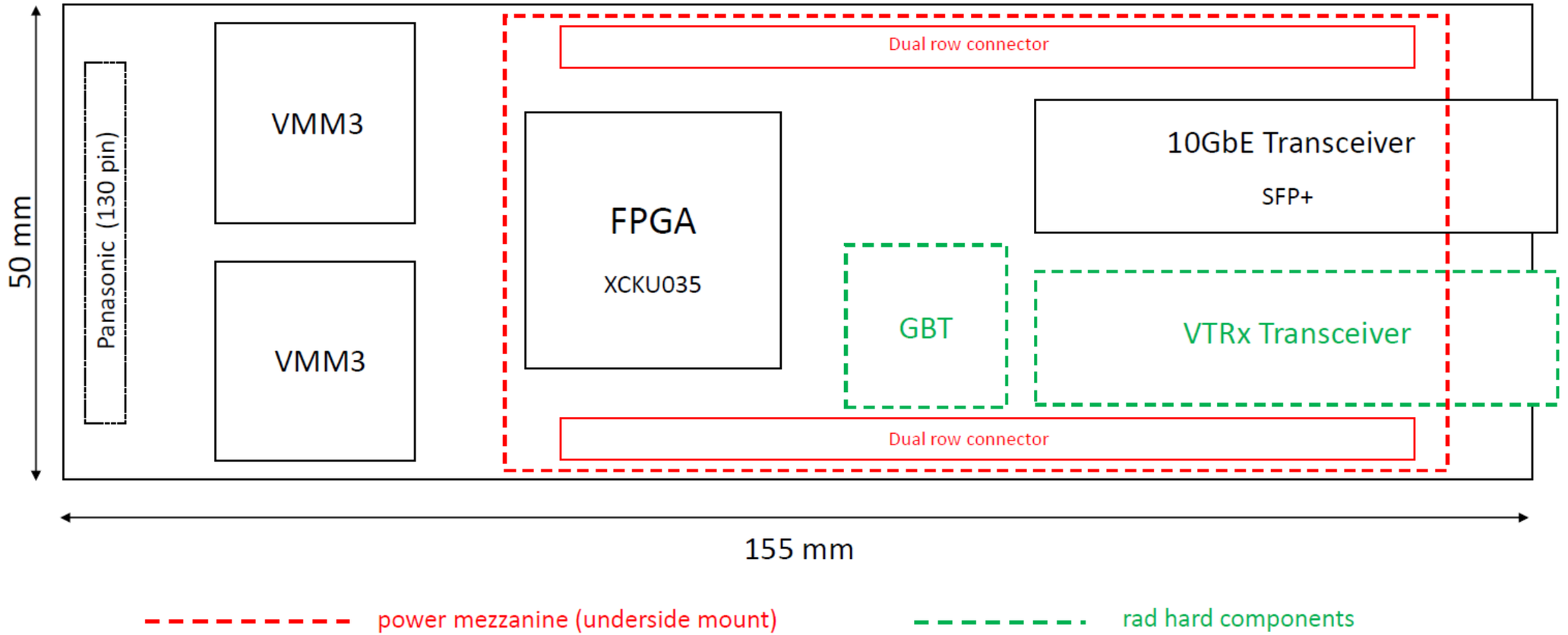
Figure 4: Top view of the FEASTMP module with mechanical dimensions.

Figure 3: Side view of the FEASTMP module with mechanical dimensions.

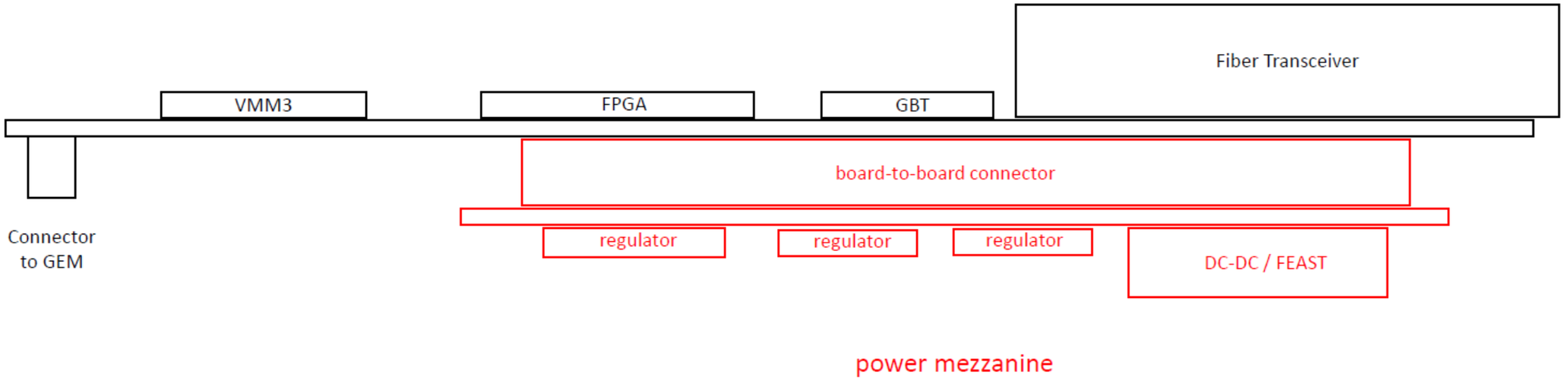
- Modules take up a large area of board space
- Many tests of the prototype and detector don't need rad hard power components

- Solution: place all power components on a *power mezzanine* board
  - Many pin connector assures low resistance, low inductance between boards
  - can build a COTS version now and replace it on the prototype with a FEAST version when needed
  - can build a version that just accepts cables from a remotely located power supply

VMM3 Prototype Board



VMM3 Prototype Board



VMM3 Prototype Board Status and Plans

- PCB design well underway
- Layout of PCB and routing of signals between VMMs and FPGA (Jeff Wilson, FE-DAQ group)
- Thanks to ATLAS collaborator USTC (China) for giving us the CAD file for their production version of the sTGC front-end card. From it we extracted the CAD model of the VMM3 chip as well as information about the layout (power, ground) for the sensitive mixed-signal VMM3 chip.
- FPGA firmware design started (no redundancy). VHDL code for 10GbE interface already exists (Ben Raydo, FE-DAQ).

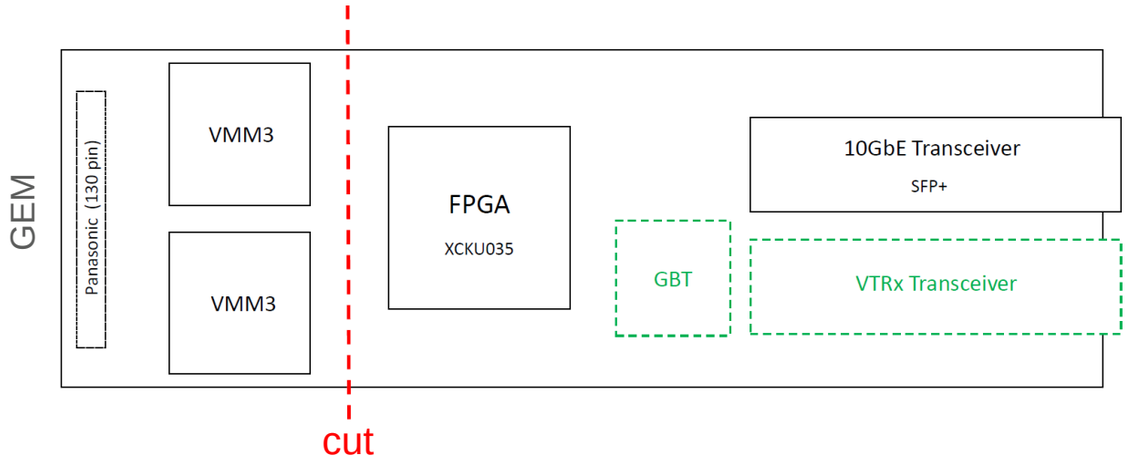
- Planned high-rate x-ray tests at University of Virginia with10GbE readout, COTS power (fall 2020)
- Integrate FELIX PCI-e readout card into JLab DAQ software (fall 2020)
- Triple Modular Redundancy firmware (early 2021)
- Rad hard power mezzanine; radiation tests with FELIX readout (spring 2021)

Options for VMM3 Readout Card

(1) Connect GEM to readout card with cable. Locate readout card in lower radiation zone.

(2) Split readout card into 2 pieces

- carry digital signals across with cable or flex circuit
- locate section with FPGA in lower radiation zone



(3) Convert FPGA design into rad hard ASIC

- initiated contact with designers of the ROC ASIC (Transilvania University) and TDS ASIC (University of Michigan) to find out about the process and cost (both are digital designs for the ATLAS New Small Wheel)
- the ROC ASIC is closest to our design (TDS has multi-GHz data serialization)

VMM3 Evaluation Boards

- Acquired 2 VMM3 evaluation boards (MMFE1, GPVMM3) during JLab shutdown
- Set up Linux virtual machine (VirtualBox) at home on Windows 10 PC to run VMM configuration and acquisition software (VERSO)
- Able to configure VMM on evaluation board and acquire data using built in pulser of VMM chip (normal data path)
- Data has problems – no scope available to look at diagnostic outputs on board
- Project paused to get high-speed VMM readout prototype started
- Now have later version of the VERSO software
- Work in progress …

- One evaluation board (MMFE1) will be connected to GEM detector in Hall A during upcoming run and will be read out using VERSO software in high radiation environment

VMM3 Evaluation Boards

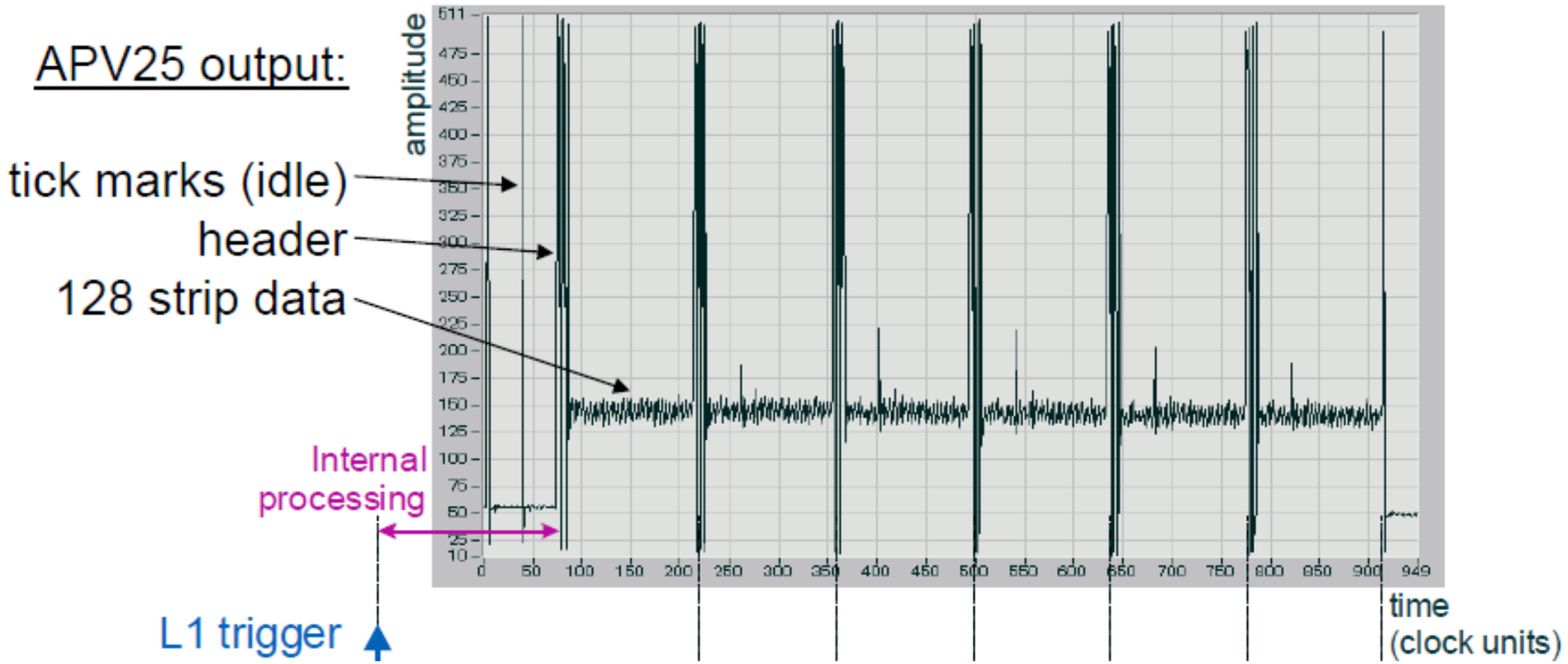
- The GPVMM3 evaluation board routes the direct outputs of **12 VMM3 channels** to a connector
- We will cable this connector to an Xilinx FPGA evaluation board to read out the 6-bit ADC data (no hardware to design)
- The FPGA on the Xilinx evaluation board is from the *UltraScale* series and so can natively receive the low level SLVS signals that the VMM3 outputs
- We will read out the FPGA evaluation board using 1GbE, so high-rate operation is possible. VHDL code for 1GbE interface already exists (Hai Dong, FE-DAQ).
- Firmware development required – this code can be reused in the prototype design
- This will give us a first look at the VMM3 direct outputs

APV25 preRD

- APV25 is a 128 channel pipelined analog sampling chip with trigger buffering
- In peak mode **1 sample** per channel per trigger
- 141 analog data per trigger (128 channels + header + error flag)
- 40 MHz clock: 141 x 25 ns = 3.6 us per trigger
- APV25 should be able to handle up to 278 KHz average trigger rate (peak mode)
- *N* samples per channel can be obtained by applying *N* chip triggers on consecutive clock cycles for every physics trigger. Max trigger rate = 278 / *N.* (Caution: buffer overflows)
- Need to optimize read out for maximum data throughput

APV25 preRD

Single L1 trigger resulting in 6 samples



GEM – Readout Electronics

- 128 analog ch / APV25 ASIC
- 3.4 μs trigger latency (analog pipeline)
- Capable of sampling signal at 40 MHz
- Multiplexed analog output (100 kHz readout rate)

	Channels	APV25	MPDs
Front Tracker	28000	216	16
Rear Tracker	12000	100	7

MPD (INFN)

05/Aug/2019

MPD Main Block

Arriga GX FPGA
128 MB DDR2-RAM
Firmware V4.0 (74% resources):
FIR Filter (16 param)
Zero Suppression
Common mode and pedestal subtraction
Remote config,
≈2 ns trigger time resolution

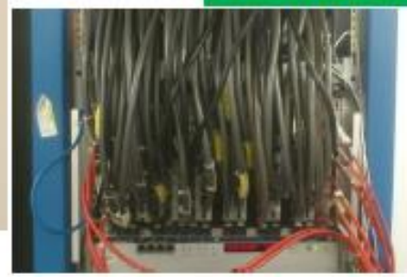
MPD-SSP Interface → SSP-Protocol → Aurora Protocol

MPD-VME Interface → VME-Protocols → 2eSST, 2eVME, VME32 ..., VXS

Optical Fiber

VME (64x)

All major firmware issues fixed so far



Electronics is up and running (or going to run) on:

- Front-GEM cosmic test in VME mode
- SSP mode in Rear GEM cosmic test
- PREX UVa GEM

MPD optical readout development

- Use optical link to read MPD allows readout in parallel of modules : bandwidth = 32 x 125 MB/s vs VME = 200 MB/s
- SSP readout up to 32 MPD per SSP
- Zero suppression scheme on SSP
- Still bottleneck of VME bus for SSP : 9 KHz for 6 samples for 200 MB/s

- Replace SSP by VTP readout
  - VTP readout can output to 10GbE optical fiber

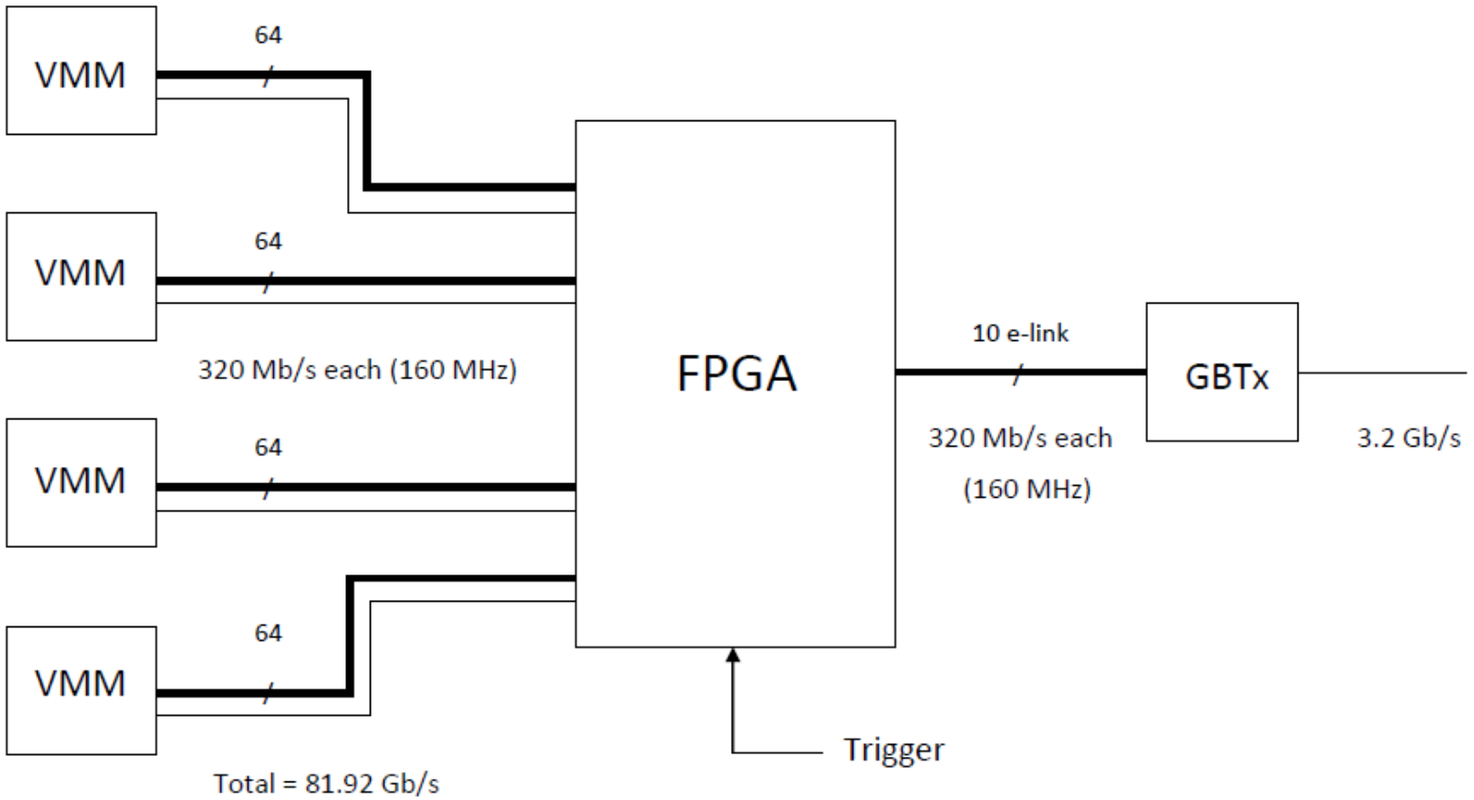
- Will be able to demonstrate 100 KHz minimum trigger rate with one sample readout

Appendix – VMM Data Rates

1 FPGA handles direct readout of 4 VMM chips

[64(channels/chip) + 1(clock/chip)] x 2(pins/signal) x 4(chips) = 520 pins (reasonable size, price FPGA)

1 GBTx data link for FPGA output data (10 e-links @ 320 Mb/s = 3.2 Gb/s)



Appendix

Data Rates

(Trigger latency < 8 μs)

For data capture window < **0.8** μs (0.8 μs = **128** x 0.00625 μs (160 MHz VMM data out clock))

r = average hit rate in channel (MHz) (assume same for all 256 channels)

w = data capture window size (μs)

Compute maximum trigger rate as a function of r, w

n = w*r = average number of hits in window

1 hit: 6 bits (ADC) + **7 bits** (time in window) = 13 bits

1 channel data (window) = 5 bits (hits in window) + 8 bits (channel number) + n*13 bits + 4 bits (status)

= 17 + n*13

all channel data (window) = 256 * (17 + n*13) = 4352 + n*3328

1 e-link header data (window) = 32 bits (trigger timestamp) + 16 bits (event number) + 8 bits (other)

= 56 bits

header data (window) = 56 bits * 10 (e-links) = 560 bits

Total data (window) = header data + all channel data = 560 + (4352 + n*3328)

= 4912 + n*3328 bits

Appendix

Trigger rate (max) = (3200 Mb/s) / (4912 + w*r*3328 b)

e.g. r = 10 MHz, w = 0.400 μs => Trigger rate (max) = 176 KHz

r = 15 MHz, w = 0.400 μs => Trigger rate (max) = 129 KHz

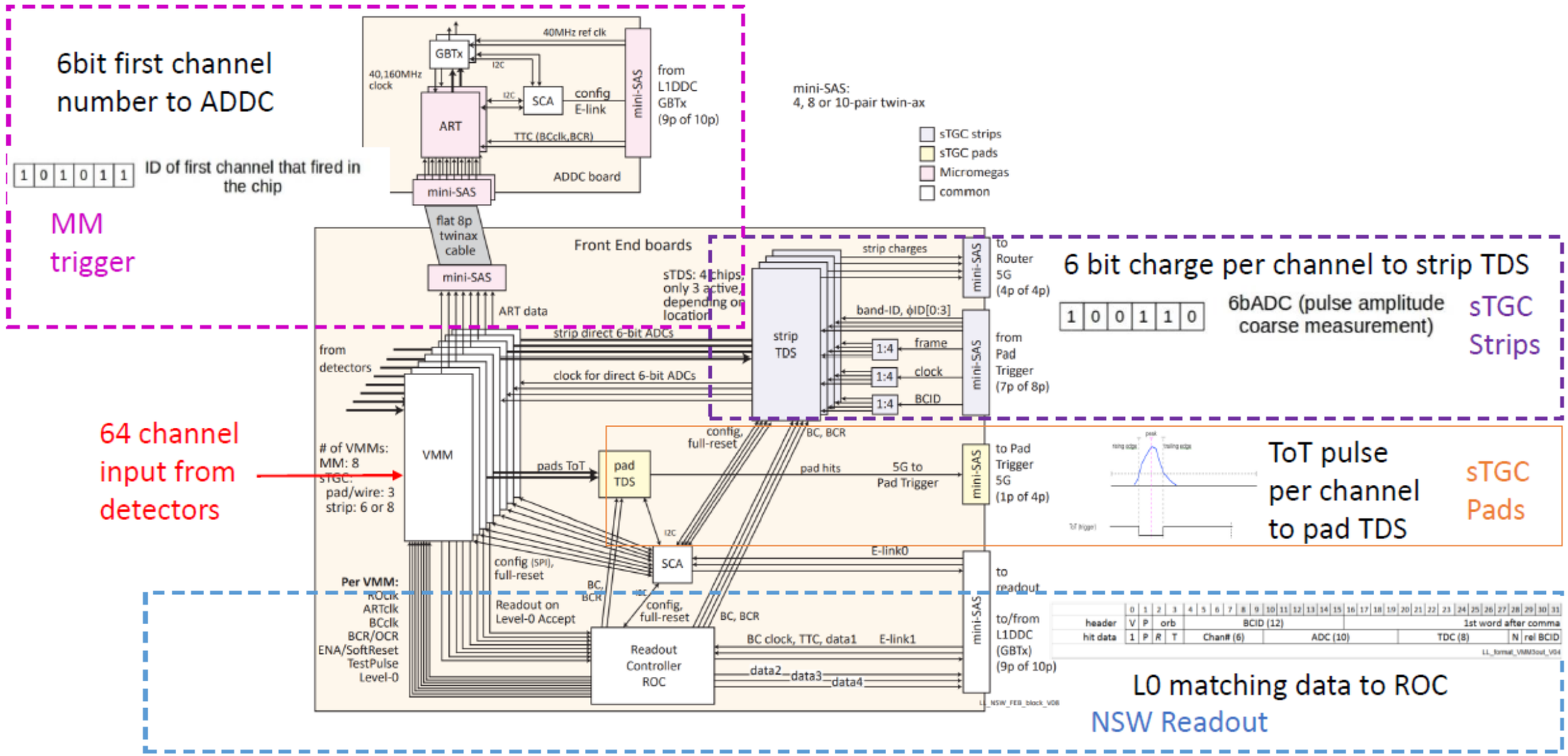
Or we can solve for the quantity w*r:

R = trigger rate (MHz)

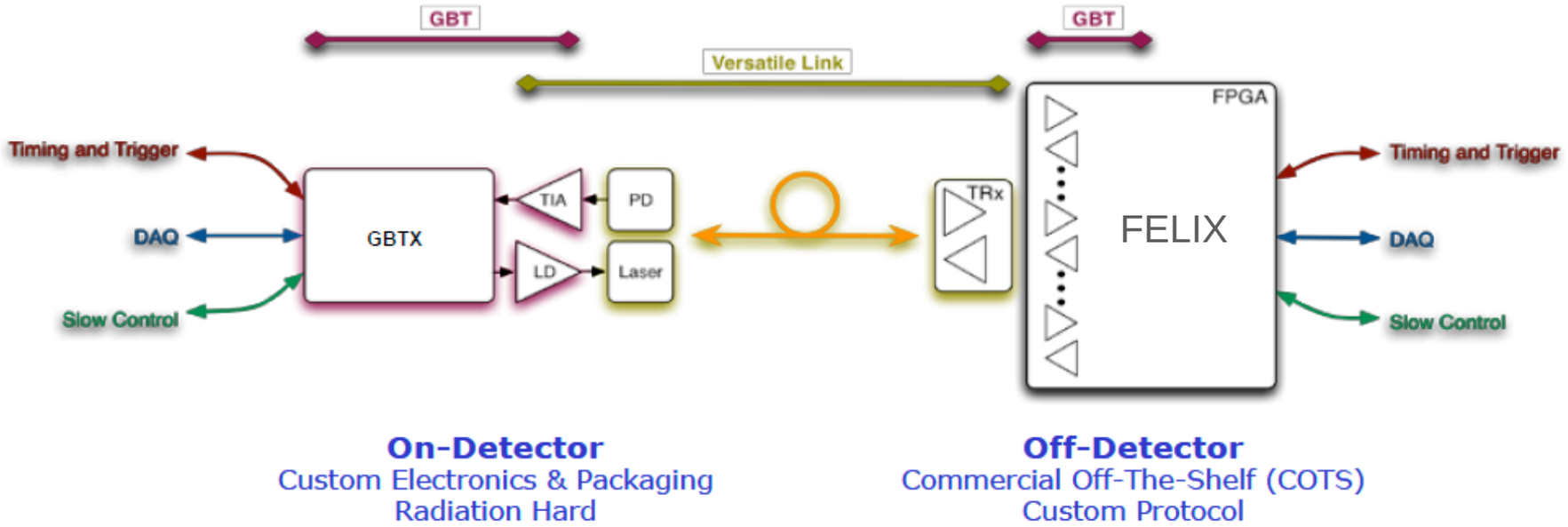
w(μs)*r(MHz) = 1.04166 / R(MHz) - 1.51563

REFERENCE SLIDES

VMM Interface



GBT - VTRx link

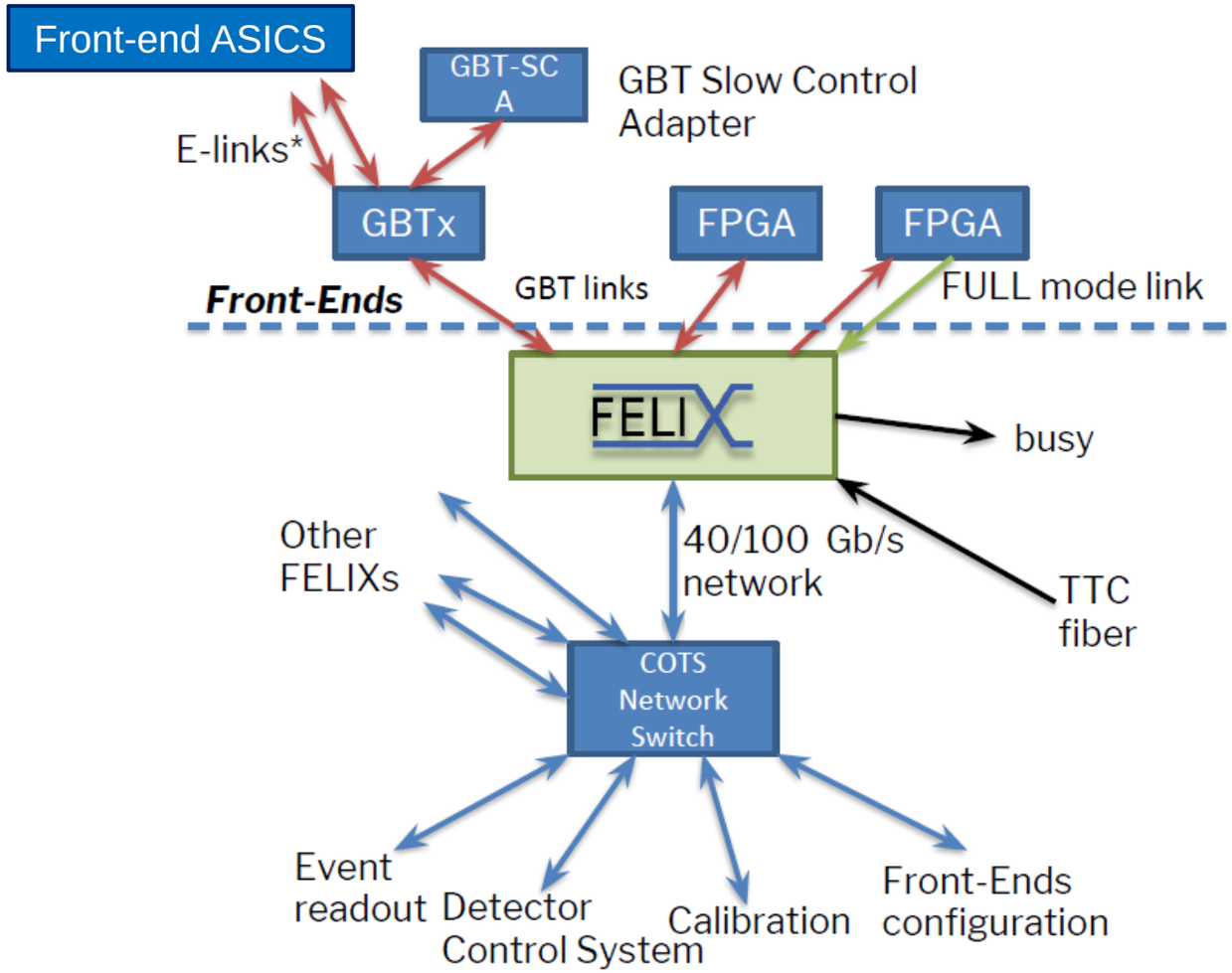


Single bidirectional rad hard optical link simultaneously provides data paths for:

- Timing and Trigger Control (TTC)
- Data Acquisition (DAQ)
- Slow Controls (SC) – configuration and monitoring

<u>Fixed Latency</u>

FELIX

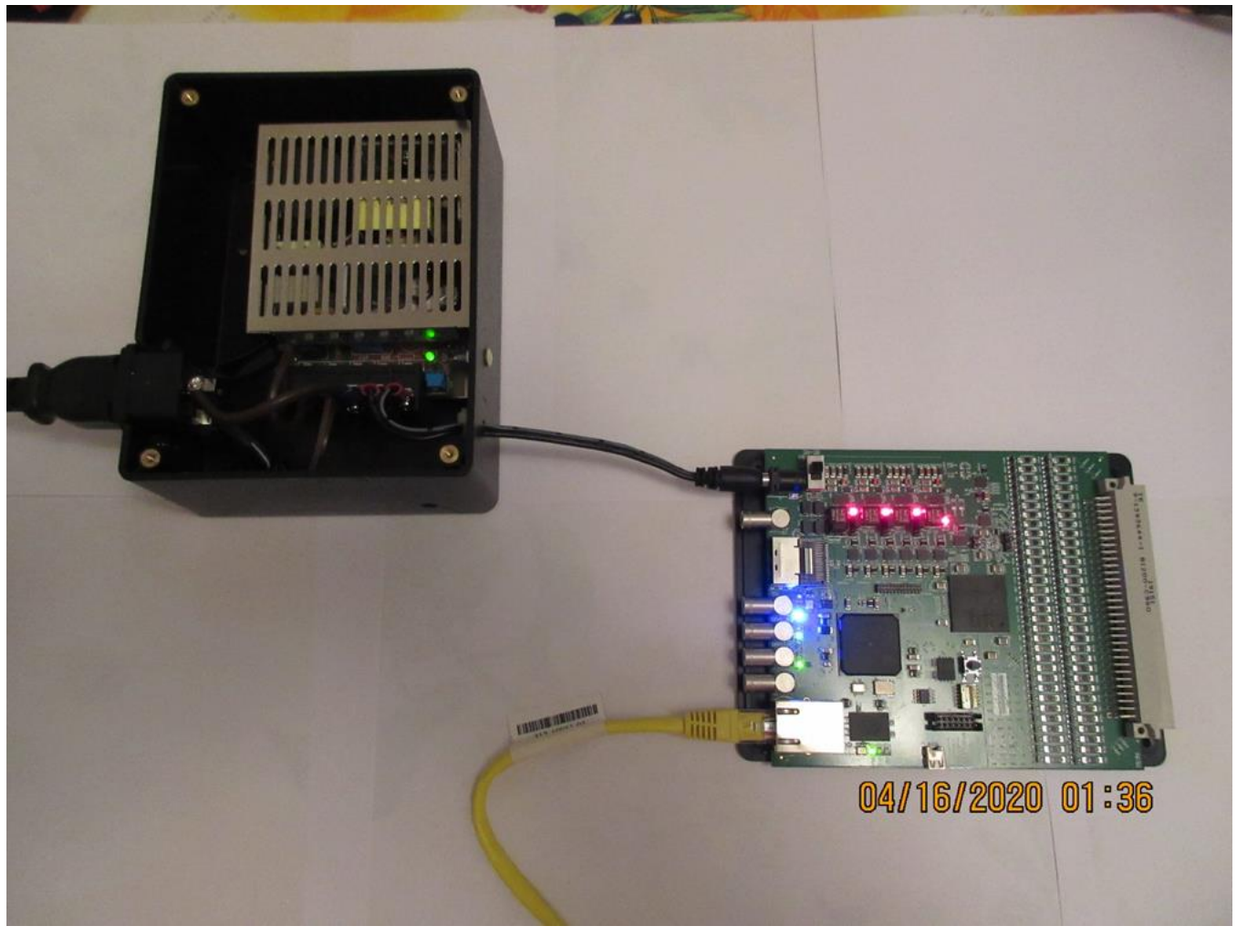


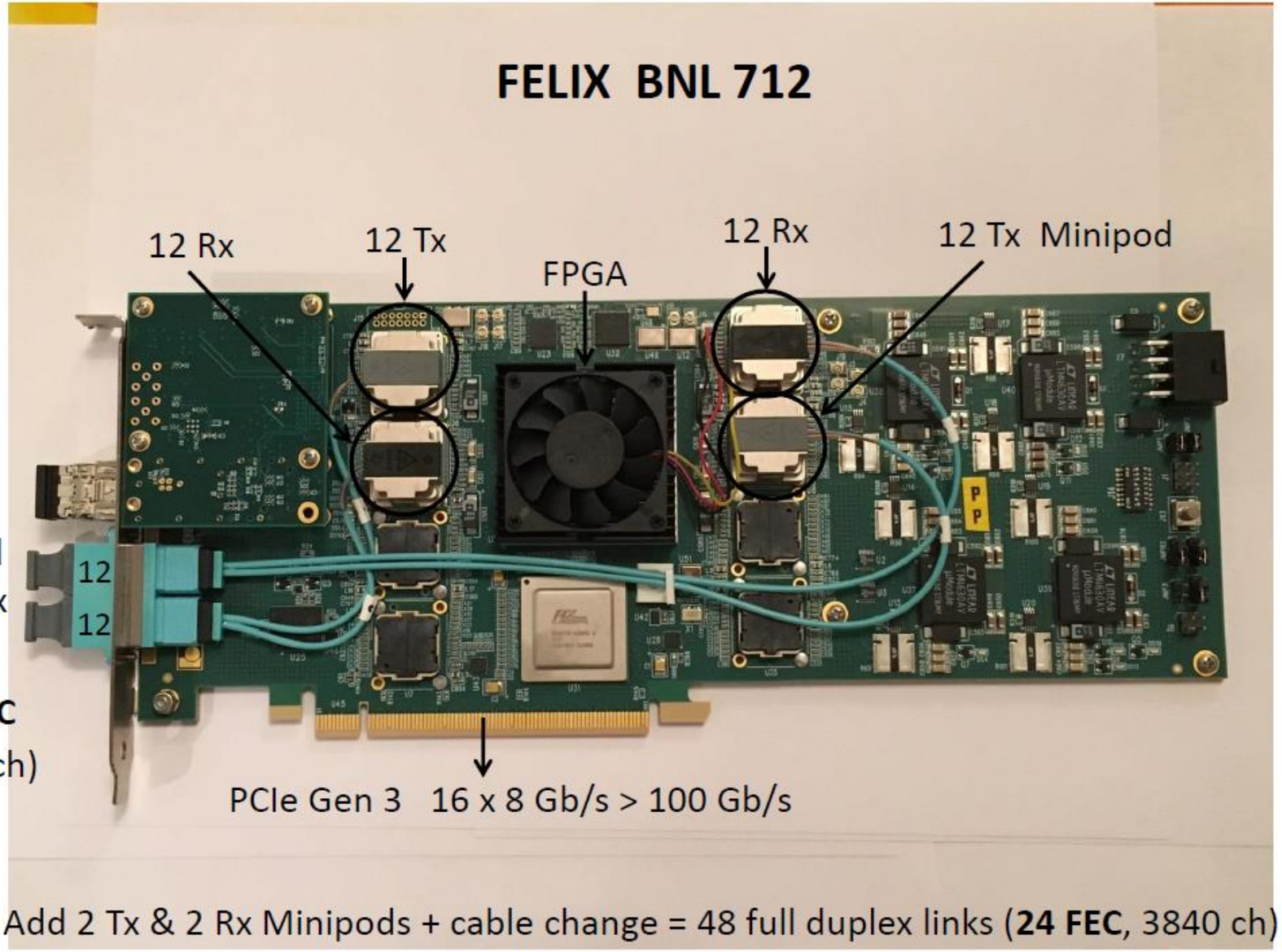
- FELIX is a router between front-end serial links and a commodity network, which separates data transport from data processing.
- Routing of detector control, configuration, calibration, monitoring and detector event data
- TTC (Timing, Trigger and Control) distribution integrated
- Configurable E-links in GBT Mode
- Detector independent

FELIX hardware implemented in PCIe Gen3

VMM3 Evaluation Board

- With home made power supply during JLab shutdown




FELIX BNL 712
12 Rx
12 Tx
FPGA
12 Rx
12 Tx Minipod
24 full duplex links
12
12
12 FEC
(1920 ch)
PCIe Gen 3 16 x 8 Gb/s > 100 Gb/s
Add 2 Tx & 2 Rx Minipods + cable change = 48 full duplex links (24 FEC, 3840 ch)