Jefferson Lab

GlueX-doc-1364

The GAS-II/GPC-II GlueX Preamp Card Preliminary Test Results

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1. Introduction

This report describes the test results obtained from the new 24 channel preamplifier card (GPC-II) for the GlueX experiment in Hall D at Jefferson Lab. These tests were performed to verify the operation of fully populated boards with the new GAS-II ASIC. For information on the previous version of the preamp card, please also refer to GlueX-note-871.

2. The GAS-II ASIC

The GAS-II ASIC was developed based on the results obtained from the previous version of the ASIC (GAS-I) with detector prototypes and to satisfy the requirements of both the CDC and the FDC. Two amplification settings are now available: the low gain setting is selected to be used with the anode wires on the CDC and the FDC; the high gain setting is to be used with the FDC micro-strip cathodes. A leading-edge discriminator has also been designed into the ASIC and this is selected for use with the FDC anode wires.

A number of configuration pins, i.e. bits, determine the operation of the ASIC (appendix A) such as the shaping constant, gain and enabling of the comparator. Some of these combinations also impact the power consumption.

3. The GPC-II Preamp Card

The GlueX Preamp Card (GPC-II) was designed to be employed with both Hall D wire chambers: FDC and CDC. The GPC-II can be configured for either anode or cathode readout, with various gain and shaping settings and with either analog or discriminator outputs.

There will be three production assembly variants as outlined in table 1:

Table 1 – GPC-II Assembly Variants

GPC-II Variant	Application	# Ch	# Cards (24-Ch)
V1	FDC Anodes	2304	96
V2	FDC Cathodes	10368	432
V3	CDC Anodes	3500	152

The three assembly variants will be nominally configured as follows:

V1 – Input = Anode Readout
Gain = 0.6 mV/fC
Outputs = Discriminators.

V2 – Input = Cathode Readout
Gain = 3 mV/fC
Outputs = Analog.

V3 – Input = Anode Readout
Gain = 0.6 mV/fC
Outputs = Analog.

Figures 1 and 2 show the top and bottom, respectively, of the preamp card and as received from assembly.

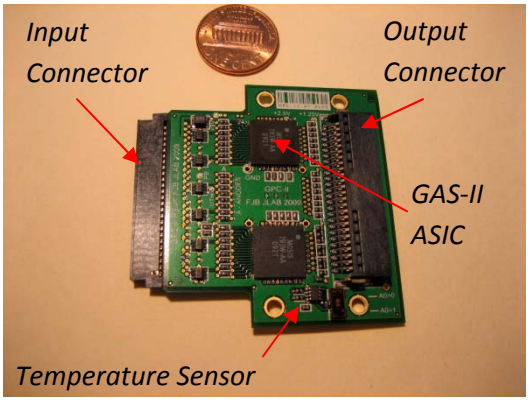


Figure 1: GPC-II – Top View.

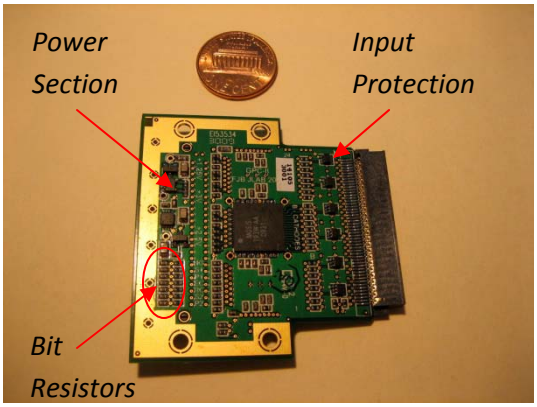


Figure 2: GPC-II – Bottom View.

4. Test Setup

A short-pulse charge injector, as depicted in figure 3, was used to test all the 24 preamp channels. The test setup is shown in appendix B.

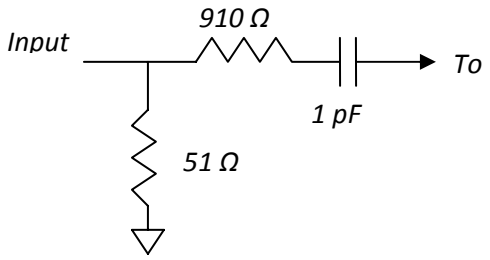


Figure 3: Short –Pulse Charge Injector

Except as indicated, all the tests were performed with the ASIC bits set at their default values and with the outputs referenced to +1.25V through 56 Ω resistors. The standard GlueX output drive configuration is shown in appendix C, where RTERM differentially terminates the complementary outputs. Note that the cable specified for use with the CDC and the FDC has a characteristic impedance of 100 Ohm.

5. Linearity

The impulse response was measured for varying input charges. Figure 4 shows the response to 100 fC of charge for the low gain configuration with the following bit configuration:

INPA1=INSH1=SH_RC=0,
INPA2=INSH2=1

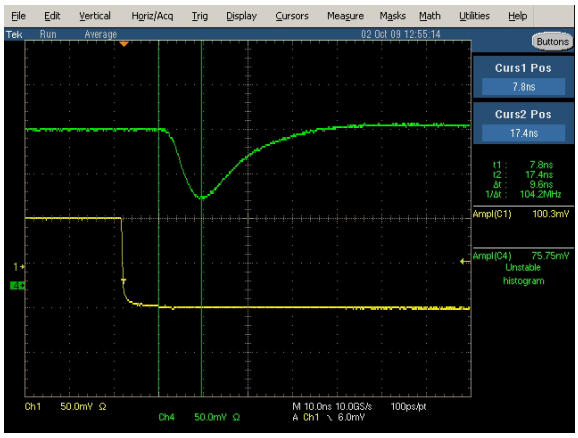


Figure 4: Impulse response to 100 fC.

The differential output is shown in green and the input step (yellow) amplitude corresponds to 100.3 fC. The peaking time is 9.6 ns.

Figure 5 shows the response under the same conditions for each of the complementary outputs. The A output (purple) has a baseline of 1.27V; the B output has a baseline of 1.17V. These values are expected to vary slightly from channel-to-channel and from chip-to-chip and are due to process tolerances during fabrication of the ASIC.

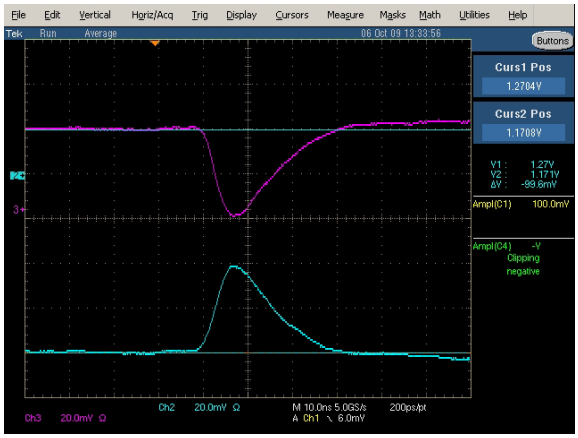


Figure 5: A & B outputs to 100 fC.

Figure 6 shows the response to 400 fC of input charge with the following bit configuration:
INPA1=INSH2=SH_RC=0,
INPA2=INSH1=1.

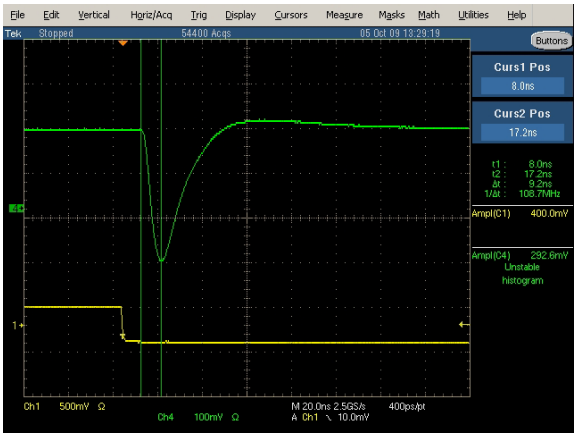


Figure 6: Impulse response to 400 fC.

Linearity plots are shown in appendix D. A summary of the relevant parameters is provided in Table 2. The bit settings are in the following order:
INPA1, INPA2, INSH1, INSH2, SH_RC, HIGAIN, EN_CMP.

Table 2 – Preamp Parameters

Bit Settings	Gain (mV/fC)	DR (fC)	Tp (ns)	P (mW)
0101000	0.77	260	9.6	49
0101100	0.57	380	12.0	49
0110000	0.85	260	8.0	54
0110100	0.62	320	11.0	54
0101010	3.2	110	10.8	49
0101110	2.6	130	13.8	49
0110010	3.6	100	10.2	57
0110110	2.9	120	13.0	57
0100000	0.69	230	9.6	46
0111000	0.91	260	8.6	56

The gain was obtained from linear fits for input charges up to 100 fC; the linear dynamic range was

determined at a level of 5% deviation from the linear fits; the peaking time was measured at 50 fC of input charge; and the power dissipation is shown for each preamp card channel.

6. Discriminator

The discriminators are enabled by setting EN_CMP=1 and can be operated in either low or high gain configurations. The ASIC Vth line has an equivalent internal pull-up of 2 kOhm to +2.5V. The threshold voltage (Vth) is set from an externally applied low noise power supply. Figure 7 shows the comparator differential output for 2.5 fC of input charge, Vth=364 mV, low gain and default settings.

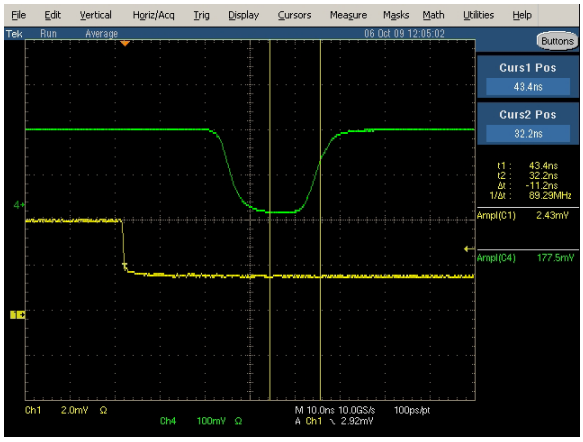


Figure 7: Discriminator output for 2.5 fC.

The low gain amplifier (top traces) and discriminator responses (bottom traces) with default settings are presented in Figure 8 for input charges of 10 fC and 100 fC and with Vth=574 mV. The time-walk is observed to be about 5 ns; the discriminator output pulse width changes from about 12 ns (10 fC) to 20 ns (100 fC); the output amplitude of the comparator is about 230 mV.

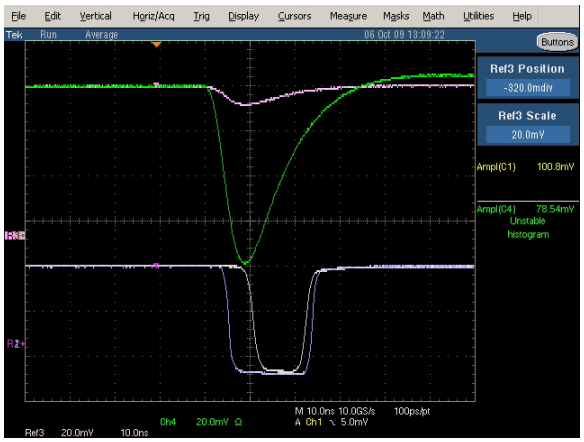


Figure 8: Time-walk for 10 fC to 100 fC.

The discriminator also behaves well for large impulse charges, low or high gain settings. This is shown in figure 9 for the high gain configuration with 400 fC and Vth=700 mV. The output pulse width increased to about 32 ns but note that this large impulse charge is not likely to occur on the FDC or CDC.

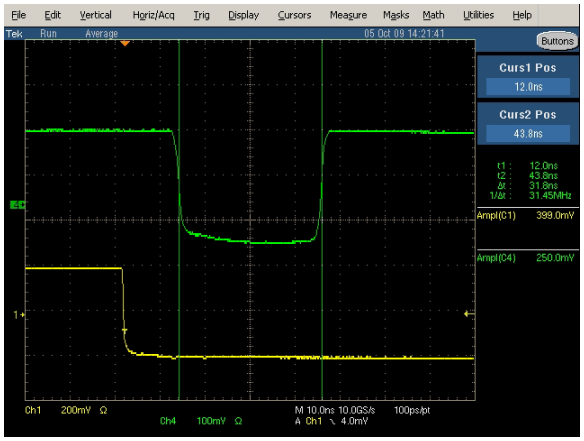


Figure 9: Discriminator output to 400 fC.

Time-walk and threshold setting plots are presented in appendix E. These

values were obtained with the amplifier set for low gain; equivalent results were observed with the amplifier set for high gain noting that the input charge was then multiplied by a factor of about 5. The threshold supply is connected to the amplifier card through a 10:1 divider formed by a series 910 Ohm resistor connected to a grounded 100 Ohm resistor (the discriminator Vth is measured at this point). A filter cap is also included.

7. Cross-Talk

The amplifier cross-talk was measured to be less than 1.2% for an impulse charge of 400 fC for the low gain configuration with the default settings. No cross-talk was observed with the discriminator in operation.

8. Noise

The noise behavior was observed on the scope by installing a 100 pF capacitor at the input of the preamp configured for low gain operation and default settings. An increase of 0.5 mVrms on the noise floor was noted but this is most likely limited by the capabilities of the scope. I estimate that the noise increase due to an input capacitance of 100pF is less than 2000 electrons referred to the input. More detailed measurements will be performed but it is clear that the noise level of the GAS-II is very good.

9. Calibration

The calibration feed to the amplifiers is differential, capacitively coupled to the A and B inputs of all 24 channels and terminated to ground (50 Ohm each). The capacitive coupling has been optimized to provide wide dynamic range while maintaining a low cross-talk figure.

Figure 10 shows a range of output pulses from the amplifier in low gain mode with INSH1=INSH2=1. External square pulses were coupled through a 1:1 pulse transformer at 1 kHz repetition rate: pulse amplitudes were 0.25V, 0.5V, 1.0V, 1.5V and 2.0V. These well behaved pulses from calibration span a range of about 250 fC. The calibration pulser is part of the fADC125 and the F1TDC and will cover the full dynamic range of the preamps, if desired.

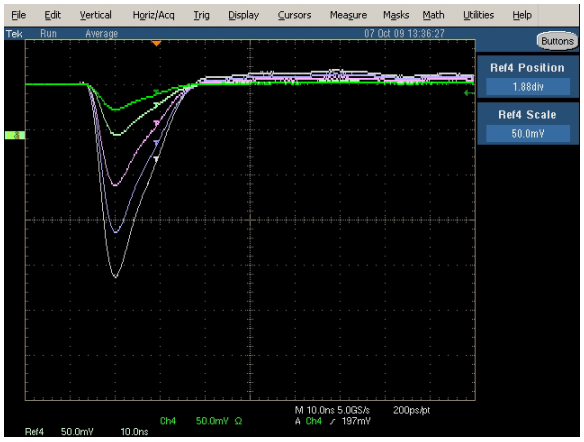


Figure 10: Output from calibration input.

10. Summary

Three fully populated preamp cards were assembled to validate the assembly processes. The quality of the assemblies was very good and no faults were observed. This is of particular importance given the QFN packaging of the ASIC. Except for changes in a few resistor values on the preamp card, the GAS-II ASIC and the GPC-II preamp card work as designed, behave well and meet the design specifications.

The two nominal gain values were specified based on tests performed with the first version of the ASIC (GAS-I): 0.62 mV/fC and 3.08 mV/fC. The values presented in table 2, together with their respective dynamic ranges and power dissipations, show that the specifications have been met. Linearity is also good for the various setting combinations but more precise measurements will be performed.

The discriminator works very well with extremely low spurious noise and good time-walk and overdrive characteristics. The discriminator has been optimized for operation with Vth set between 2 fC and 5 fC and the external threshold adjustment has a range of about 20 fC. The power dissipation is 46 mW per channel which is slightly lower than the power dissipated by the amplifier in its default setting.

Cross-talk is excellent and noise, which still needs to be characterized in detail, is low.

The calibration section has been considerably improved from the first version of the preamp card, in both dynamic range and signal quality.

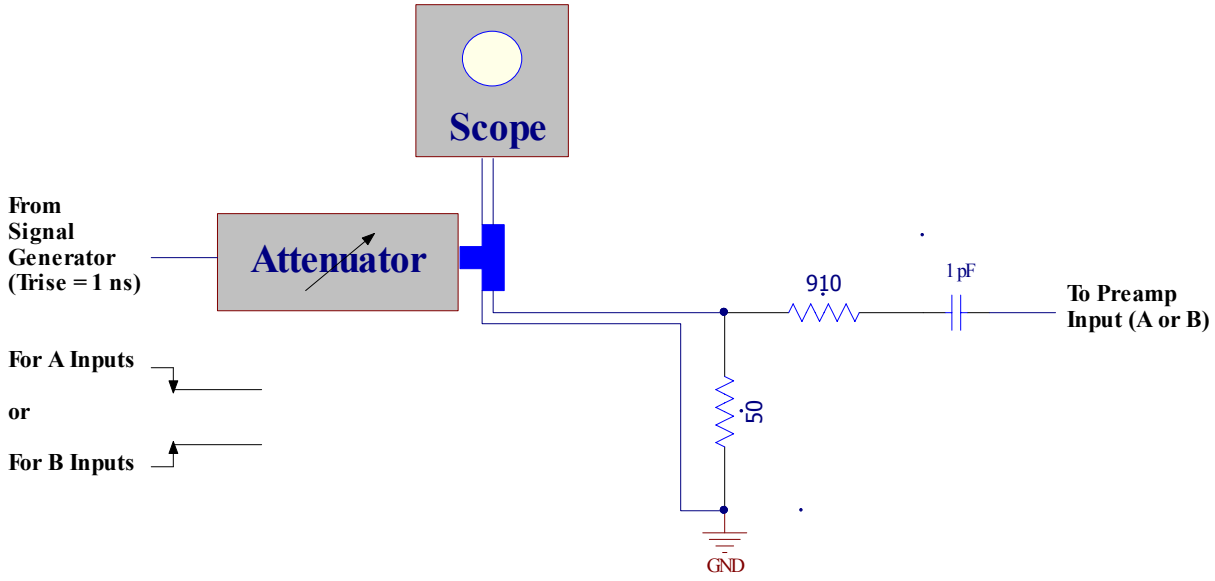
Extensive tests will be performed with the CDC and the FDC full scale prototypes to verify that the performance of the GAS-II/GPC-II preamp meets the requirements of these detectors before production can begin.

Appendix A – Configuration Bits

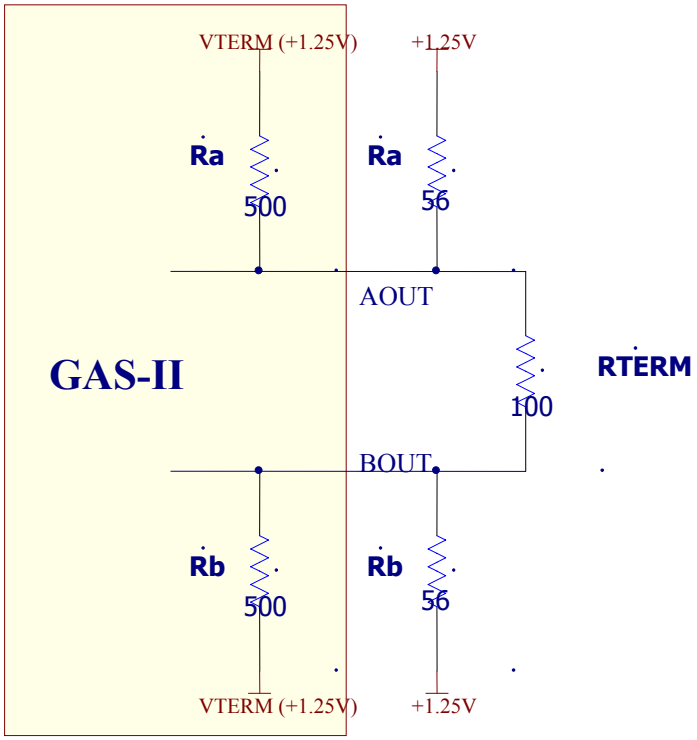
Name	Default	Function
INPA1	0	Preamp 1 current bit
INPA2	1	Preamp 2 current bit
INSH1	0	Shaper 1 current bit
INSH2	1	Shaper 2 current bit
SH_RC	0	Shape Control
HIGAIN	1	0=1X gain; 1=5X gain
EN_CMP	0	0=amplifier; 1=discriminator

Note: 0=GND, 1=Vdd (+2.5V) – Use low value resistors (0 Ohm - 5 Ohm) to change settings.

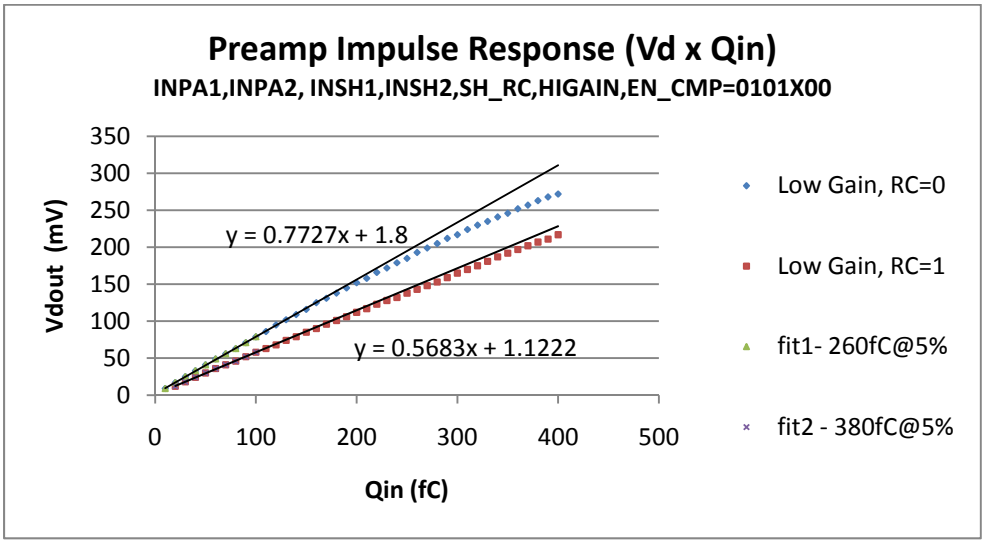
Appendix B – Test Setup

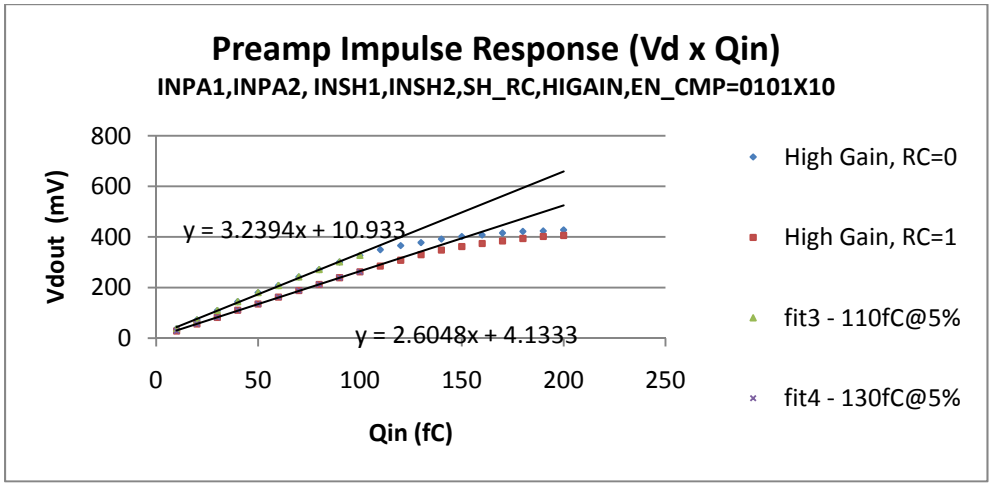


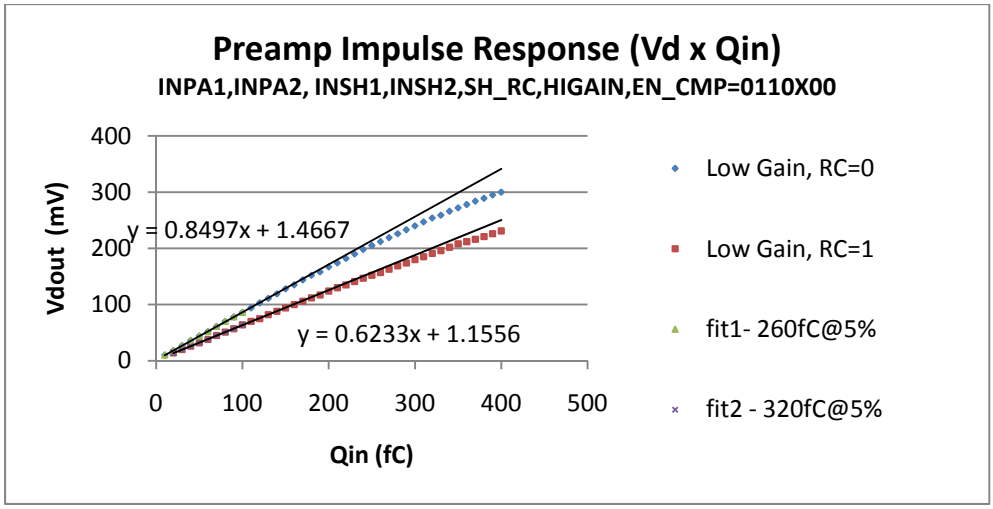
Appendix C – Output Drive Configuration

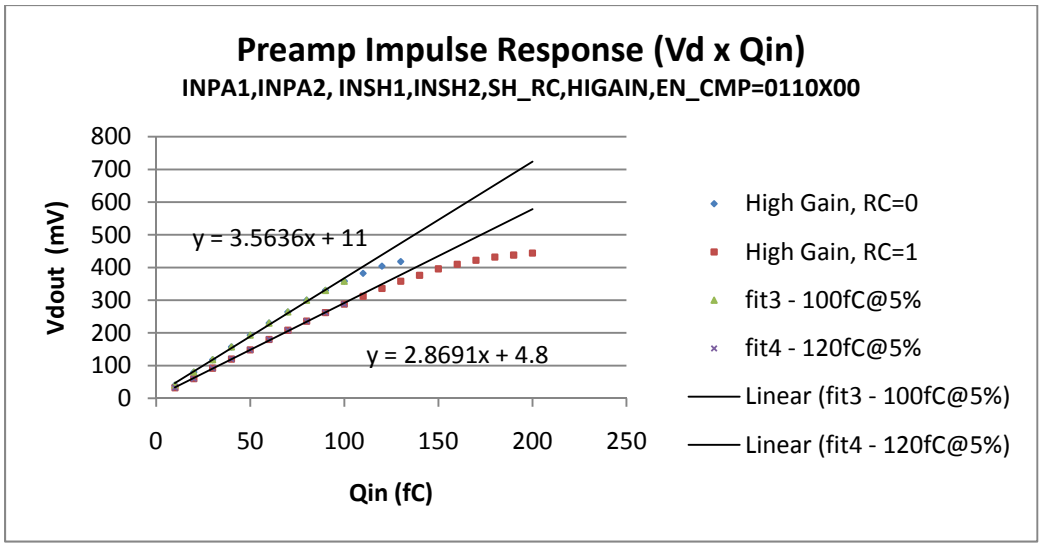


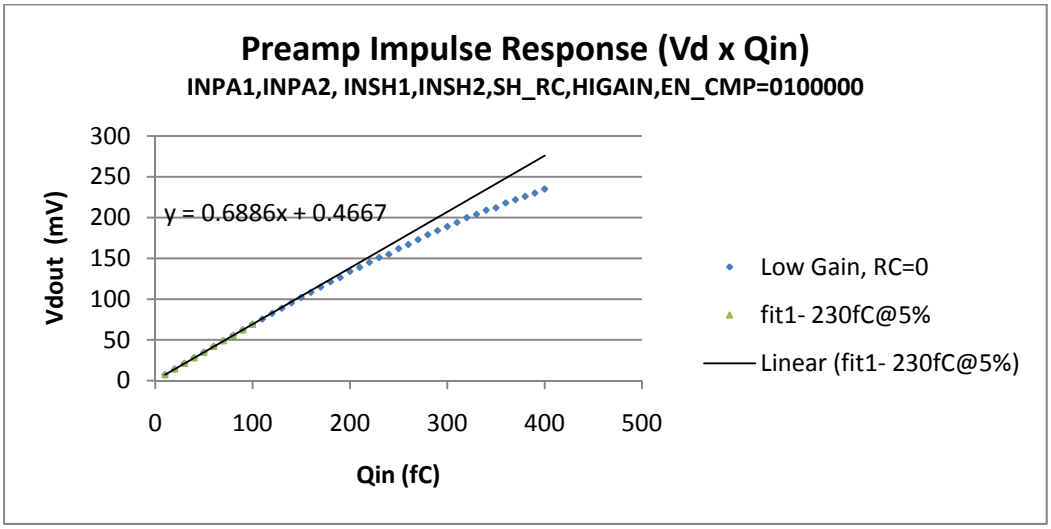
Appendix D – Linearity Plots

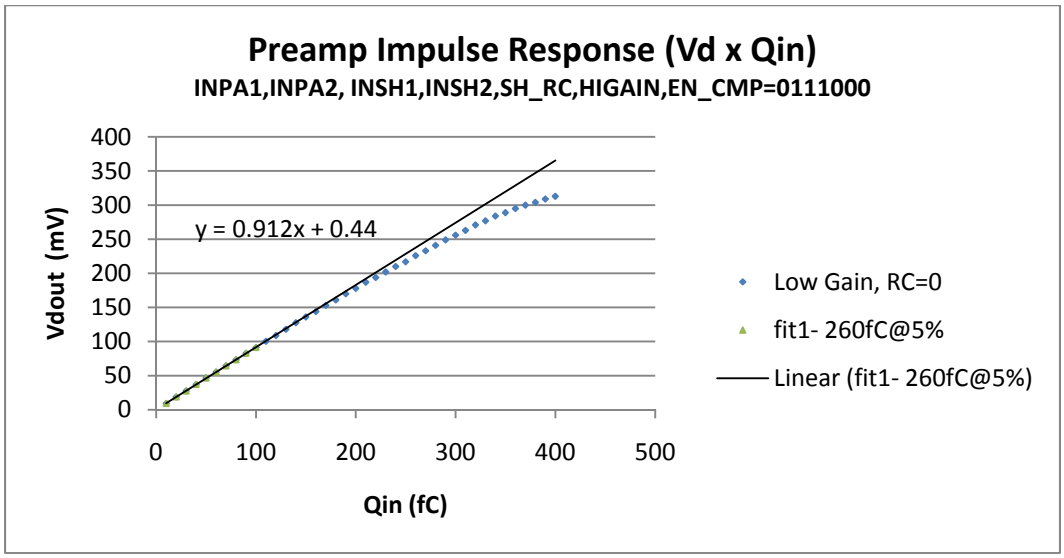







Preamp Impulse Response (Vd x Qin)
INPA1,INPA2, INSH1,INSH2,SH_RC,HIGAIN,EN_CMP=0110X00
Vdout (mV)
800
700
600
500
400
300
200
100
0
y = 3.5636x + 11
y = 2.8691x + 4.8
0
50
100
150
200
250
Qin (fC)
High Gain, RC=0
High Gain, RC=1
fit3 - 100fC@5%
fit4 - 120fC@5%
Linear (fit3 - 100fC@5%)
Linear (fit4 - 120fC@5%)


Preamp Impulse Response (Vd x Qin)
INPA1,INPA2, INSH1,INSH2,SH_RC,HIGAIN,EN_CMP=0100000
Vdout (mV)
300
250
200
150
100
50
0
y = 0.6886x + 0.4667
0
100
200
300
400
500
Qin (fC)
Low Gain, RC=0
fit1- 230fC@5%
Linear (fit1- 230fC@5%)


Preamp Impulse Response (Vd x Qin)
INPA1,INPA2, INSH1,INSH2,SH_RC,HIGAIN,EN_CMP=0111000
Vdout (mV)
400
350
300
250
200
150
100
50
0
y = 0.912x + 0.44
0
100
200
300
400
500
Qin (fC)
Low Gain, RC=0
fit1- 260fC@5%
Linear (fit1- 260fC@5%)

Appendix E – Discriminator Plots