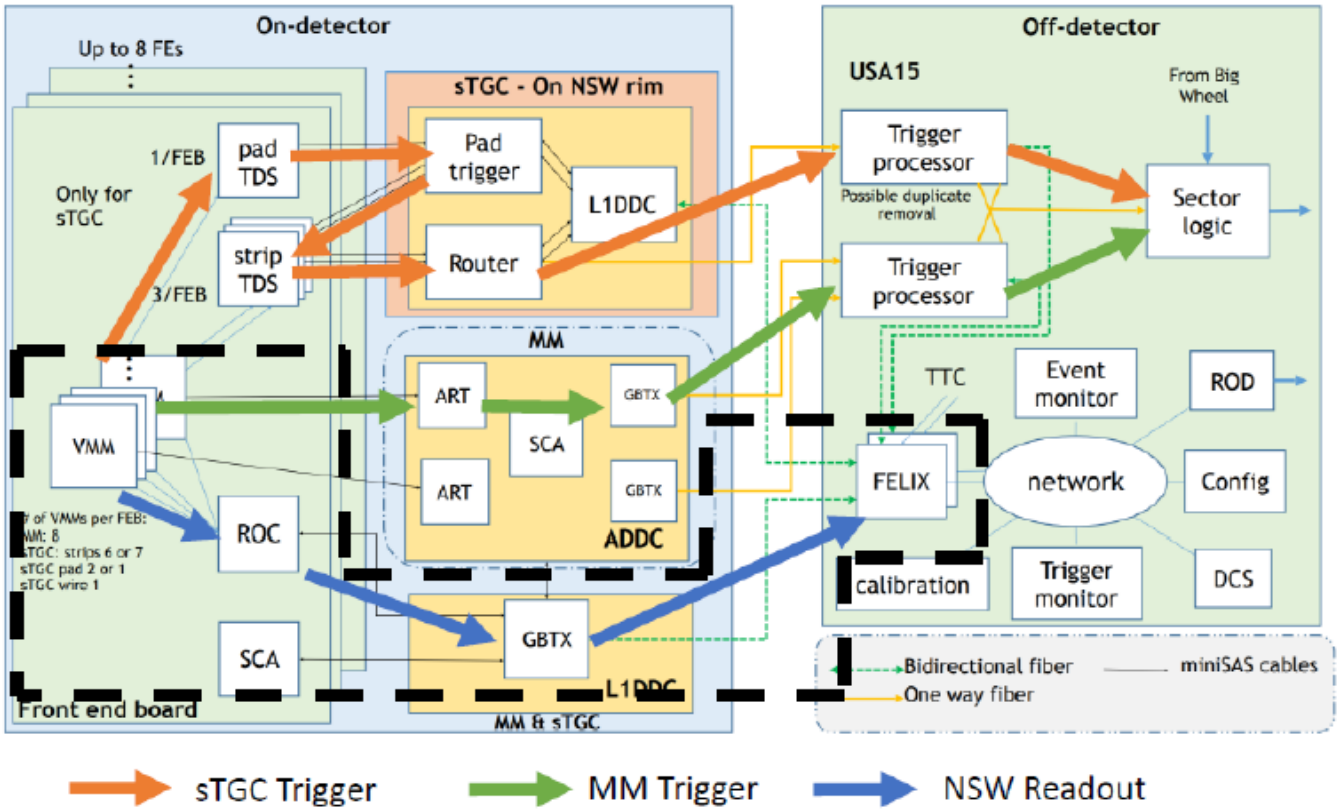
# NSW Electronics

Poster #67




Radiation tolerant ASICs:
- VMM (amplifier, shaper, discriminator)
- Read Out Controller (ROC)
- Trigger Data Serialiser (TDS)
- Address Real Time (ART)
- Slow Control Adapter (SCA)
- GigaBit Transceiver (GBTX)

PCBs:

pFEB/sFEB(sTGC pad/strip front-end board)

MMFE8(Micromegas front-end board)

L1DDC(Level-1 Data Drive Card)

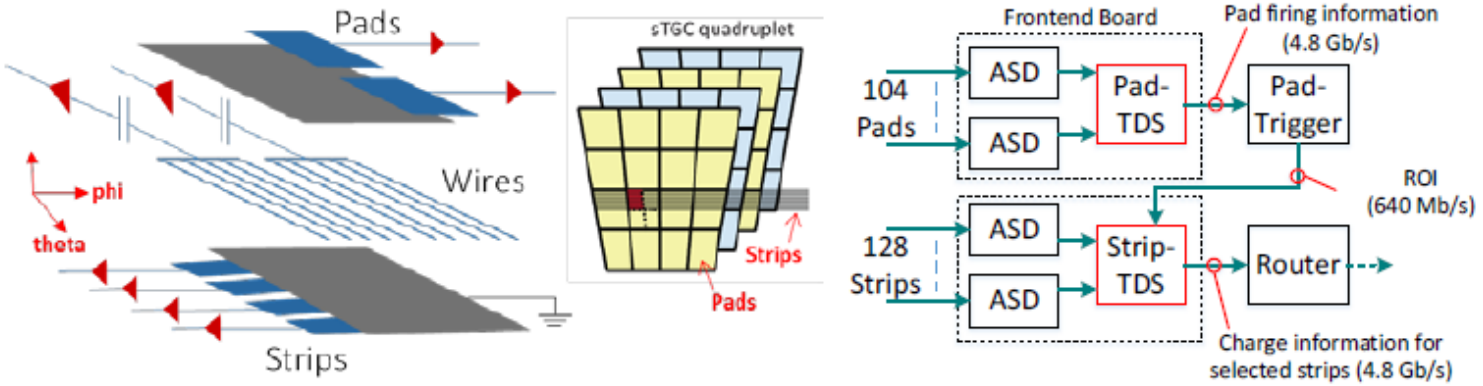
Pad Trigger

Router

ADDC

FELIX(Front-End LInk eXchange)

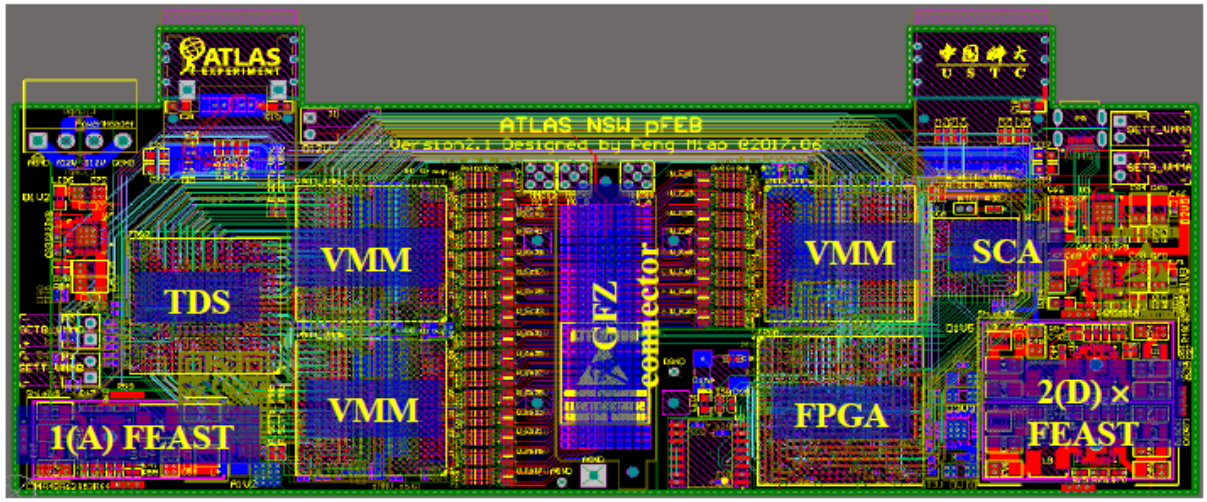
Trigger Processor




(a) (b)

Fig. 1. (a) Basic structure of the sTGC detector and an illustration of four layers of pad-wire-strip planes in an sTGC quadruplet; (b) sTGC frontend electronics chain showing TDS ASICs. See text for explanation.

# pFEB/sFEB v2.1




- Based on VMM3
- pFEB: 16.5 × 6cm, 12 layers, 192 Channels;
- sFEB: 27 × 6cm, 14 layers, 512 channels;
- Used at WZ/CERN/McGill /SDU for chamber test