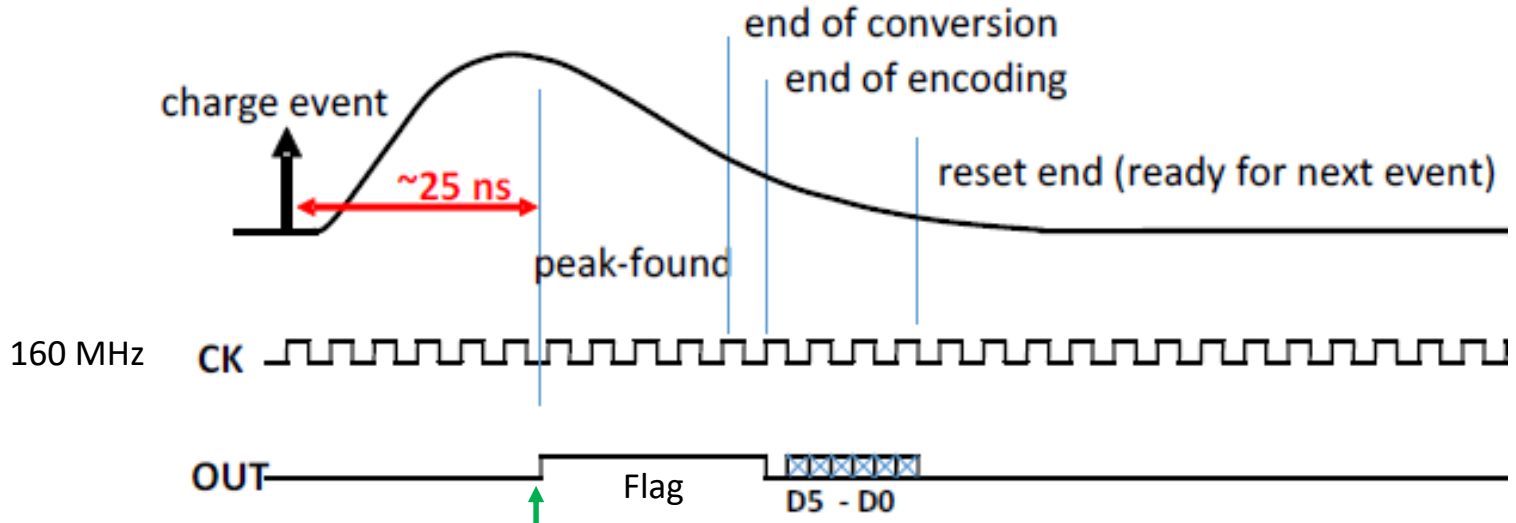
# 6-bit Direct output data format



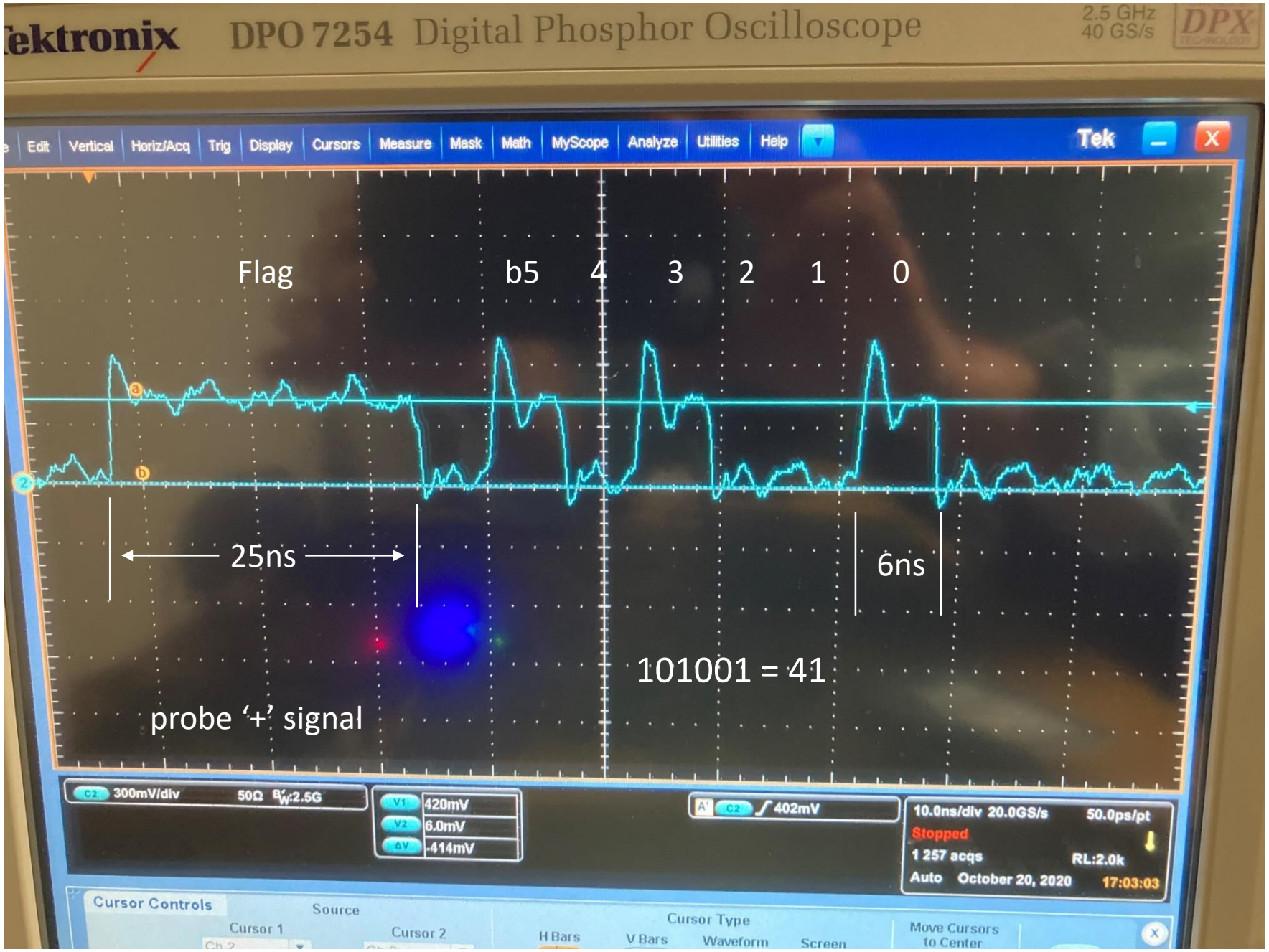

DDR - 320 Mb/s (data on both edges)

OR

SDR - 160 Mb/s (data on single edge)

400 mV

6 mV




SDR - 160 Mb/s

41 x 16 = 656

~10 bit data avg

# Xilinx Logic Analyzer on FPGA Development board - VMM Direct outputs


Sampled with 300 MHz clock