

VERSO DAQ & VMM Calibration

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NSW Electronix Weekly
Friday October 6th 2017



UNIVERSITY of CALIFORNIA
IRVINE



- VERSO Overview
- Calibration Overview
 - Procedures

- **VERSO**
 - **V**MM **E**thernet **R**eadout **S**oftware
 - Central DAQ software for:
 - Configuring VMM-based front-end boards
 - VMM2 and VMM3 in continuous or L0-trigger mode
 - Arbitrary # of front-end boards
 - (Fast) buffered, UDP based readout and event building
 - Calibration
 - Calibration runs implementing xADC-based and pulser-based calibration loops
 - Monitoring capabilities
 - It is a *graphical* interface
 - Developed alongside the baseline NSW electronics NTUA/BNL firmware
 - Hosted on NSWElectronics GitLab under [vmm_readout_software/](#)*

* will soon have the [verso/](#) repo up to date



VERSO - dev

Run Status

Run #

☒ Write Ntuple ☐ Write Raw

VMM2 VMM3 L0 R/O

Start Run
Stop Run
Calibration
Monitor
DataFlow

Setup
Config
Output /Users/dantrim
Comments

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Messages Global Registers 1 Global Registers 2 Channel Registers Calibration Set IP

Message Reporting

VERSO Info Waiting for open communication with FEB...

Bottom Verbose

FEC Response

Clear

Counters

Triggers 0
Hits 0
Event Stop -1 No Comm.

Communication

Open Communication Establish Comms

IPv4 192 168 0 2 # FEBs 1

Configure

FEB Select All Configure

VMM Select ☒ 1 2 3 4 5 6 7 8

Latency 0 x6.25ns
Dead Time 65535 x8ns
CKBC 6 **ART T/O** 24

Mode Pulser External Fixed Window
Acquisition ACQ On ACQ Off Set

CKTK & CKBC

CKTK Max 7 CKBC Freq. (MHz) 40 Defaults

CKTP

Number of Pulses to Send -1
Skew (steps) 0 x 1ns Period 30000 x 200ns
Width 4 x 500ns Defaults

Defaults Set

Monitor Sampling 50
Incidence Angle 0

FPGA Reset VMM3 Hard Reset

this is what it looks like when you start it up



VERSO - dev

Run Status

Run #

☒ Write Ntuple ☐ Write Raw

VMM2 VMM3 L0 R/O

Start Run
Stop Run
Calibration
Monitor
DataFlow

Setup

Config

Output

Comments

Counters

Triggers 0
Hits 0
Event Stop No Comm.

Communication

Open Communication Establish Comms

IPv4 # FEBs

Configure

FEB Select Configure

VMM Select ☐ 1 ☐ 2 ☐ 3 ☐ 4 ☐ 5 ☐ 6 ☐ 7 ☐ 8

Latency

x6.25ns

Dead Time

x8ns

CKBC ART T/O

Mode

Pulser
External
Fixed Window

Acquisition

ACQ On
ACQ Off
Set

CKTK & CKBC

CKTK Max CKBC Freq. (MHz) Defaults

CKTP

Number of Pulses to Send

Skew (steps) x 1ns Period x 200ns

Width x 500ns Defaults

Defaults Set

Monitor Sampling

Incidence Angle

FPGA Reset VMM3 Hard Reset

Messages Global Registers 1 Global Registers 2 Channel Registers Calibration Set IP

Message Reporting

VERSO Info Waiting for open communication with FEB...

Bottom Verbose

FEC Response

FEC response is obsolete :)

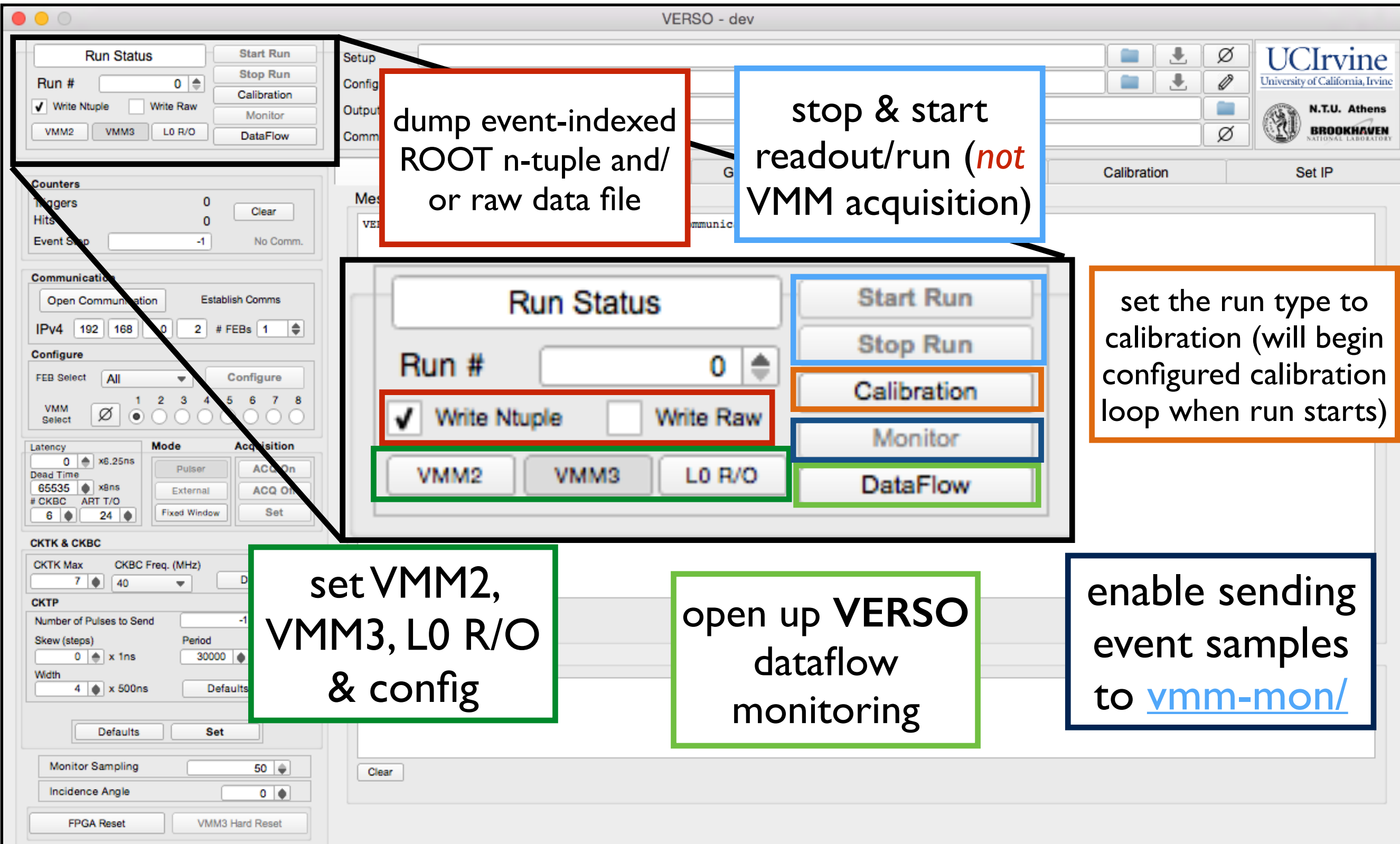
Clear

use at own risk

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useful messages appear here

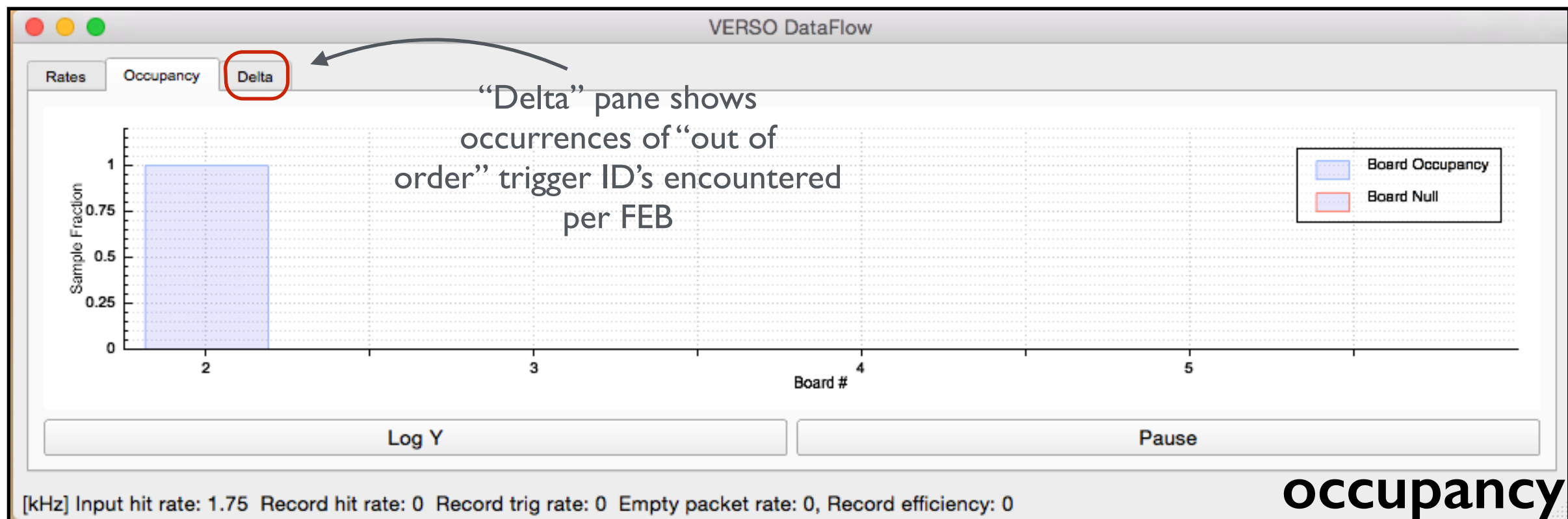
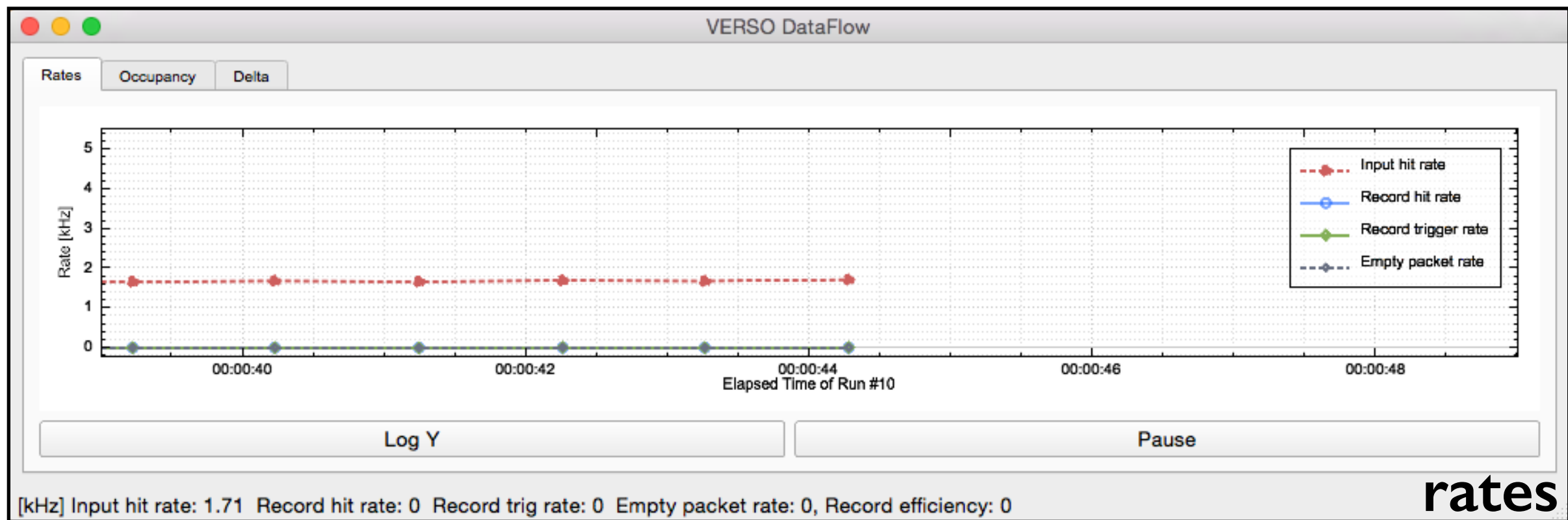


The image shows the VERSO - dev software interface with several callout boxes highlighting key features:

- Run Status** (top left): Includes Run # (0), Write Ntuple (checked), Write Raw (unchecked), and buttons for Start Run, Stop Run, Calibration, Monitor, and DataFlow.
- dump event-indexed ROOT n-tuple and/or raw data file** (red box): Points to the Write Ntuple and Write Raw options.
- stop & start readout/run (*not* VMM acquisition)** (blue box): Points to the Start Run and Stop Run buttons.
- set the run type to calibration (will begin configured calibration loop when run starts)** (orange box): Points to the Calibration button.
- set VMM2, VMM3, L0 R/O & config** (green box): Points to the VMM2, VMM3, and L0 R/O buttons.
- open up VERSO dataflow monitoring** (green box): Points to the DataFlow button.
- enable sending event samples to vmm-mon/** (dark blue box): Points to the Monitor button.

The interface also includes sections for Counters, Communication, Configure, Latency, Mode, Acquisition, CKTK & CKBC, and Monitor Sampling.

run control



dataflow window



“DAQ setup” configuration
(e.g. detector-to-elx channel
mapping, detector mapping)

VMM configuration file

Setup

Config

Output /Users/dantrim

Comments

comment/text to store as a
field inside of ROOT n-tuple

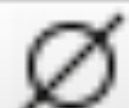
location to dump output files



file/dir look up



set/enable

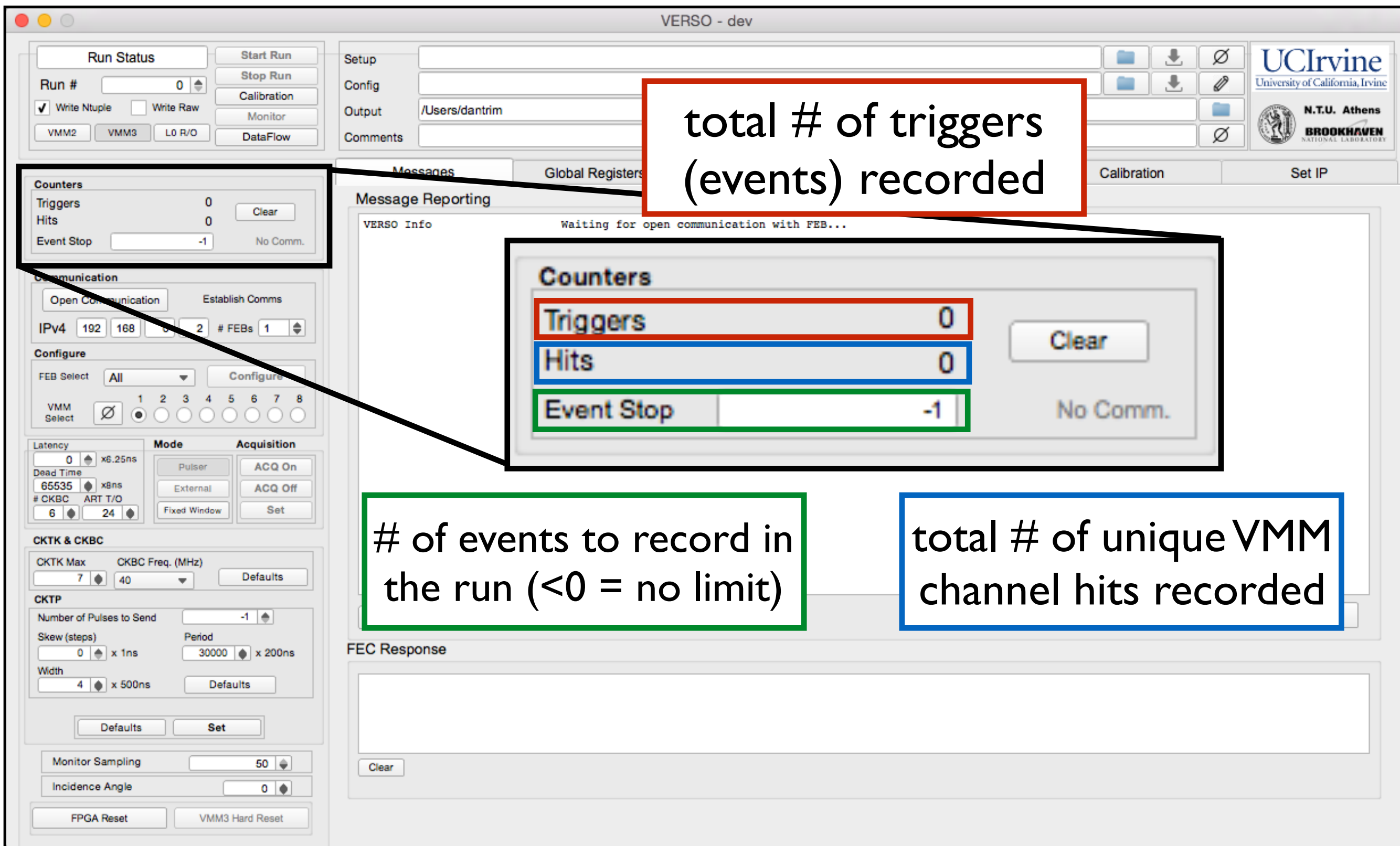


unset/disable



write config file

various top-level configuration parameters



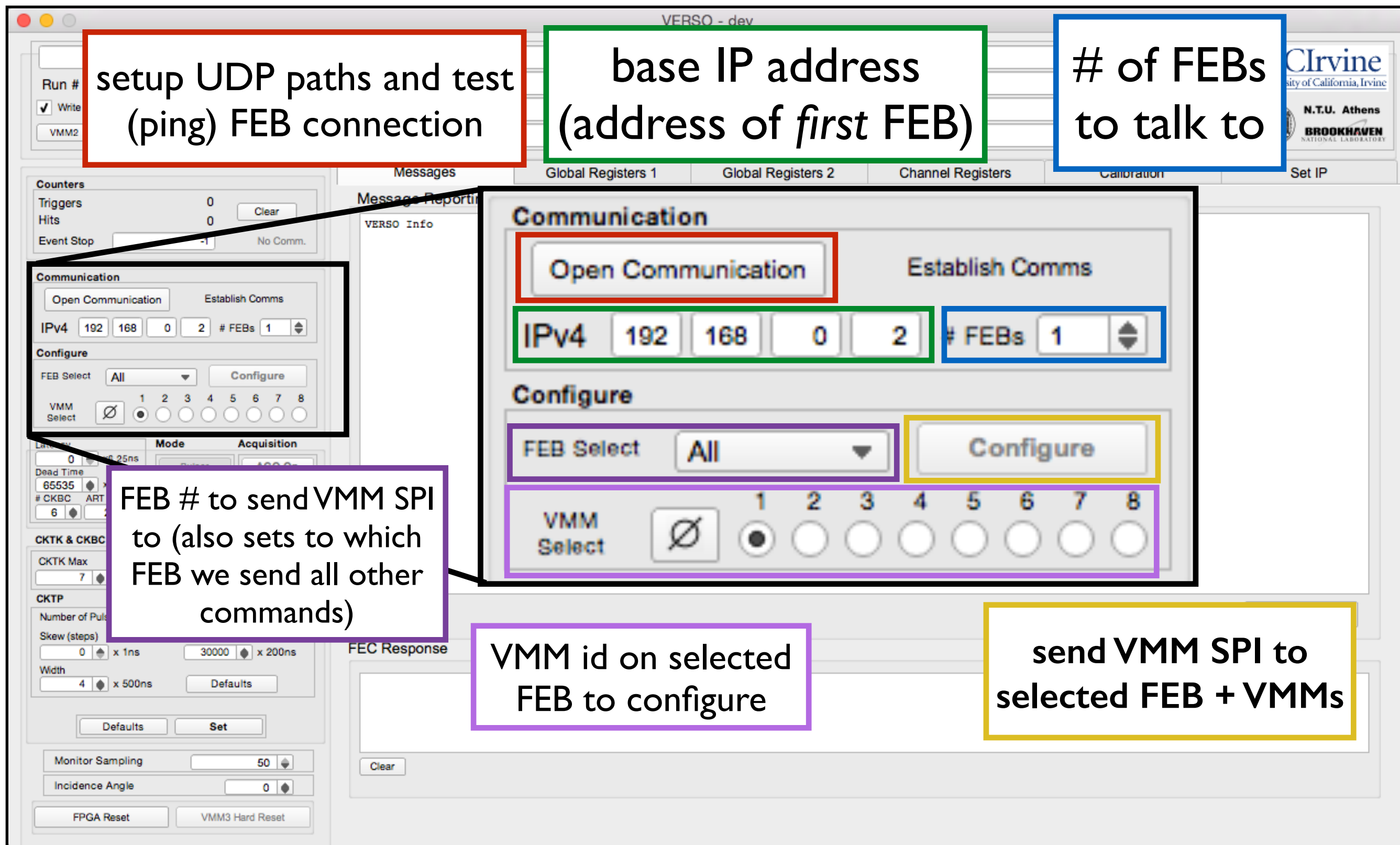
The screenshot shows the VERSO - dev software interface. The 'Run Status' section at the top left includes a 'Run #' field set to 0, 'Start Run', 'Stop Run', 'Calibration', 'Monitor', and 'DataFlow' buttons. Below this are checkboxes for 'Write Ntuple' (checked) and 'Write Raw', and buttons for 'VMM2', 'VMM3', and 'LO R/O'. The 'Counters' section shows 'Triggers' at 0, 'Hits' at 0, and 'Event Stop' at -1. The 'Communication' section has 'Open Communication' and 'Establish Comms' buttons, along with IP address and port settings. The 'Configure' section includes 'FEB Select' (set to All) and 'VMM Select' (set to 1). The 'Latency' section shows 'Dead Time' at 65535 ns and '# CKBC' at 6. The 'Mode' section has 'Pulser', 'External', and 'Fixed Window' buttons. The 'Acquisition' section has 'ACQ On', 'ACQ Off', and 'Set' buttons. The 'CKTK & CKBC' section shows 'CKTK Max' at 7 and 'CKBC Freq. (MHz)' at 40. The 'CKTP' section shows 'Number of Pulses to Send' at -1, 'Skew (steps)' at 0, 'Width' at 4, and 'Period' at 30000. The 'Monitor Sampling' is set to 50 and 'Incidence Angle' is set to 0. The 'FPGA Reset' and 'VMM3 Hard Reset' buttons are at the bottom left. The 'Message Reporting' section shows 'VERSO Info' and 'Waiting for open communication with FEB...'. The 'FEC Response' section is empty. The 'Calibration' and 'Set IP' buttons are at the top right. The 'UCL Irvine' logo is at the top right.

total # of triggers (events) recorded

of events to record in the run (<0 = no limit)

total # of unique VMM channel hits recorded

sum totals

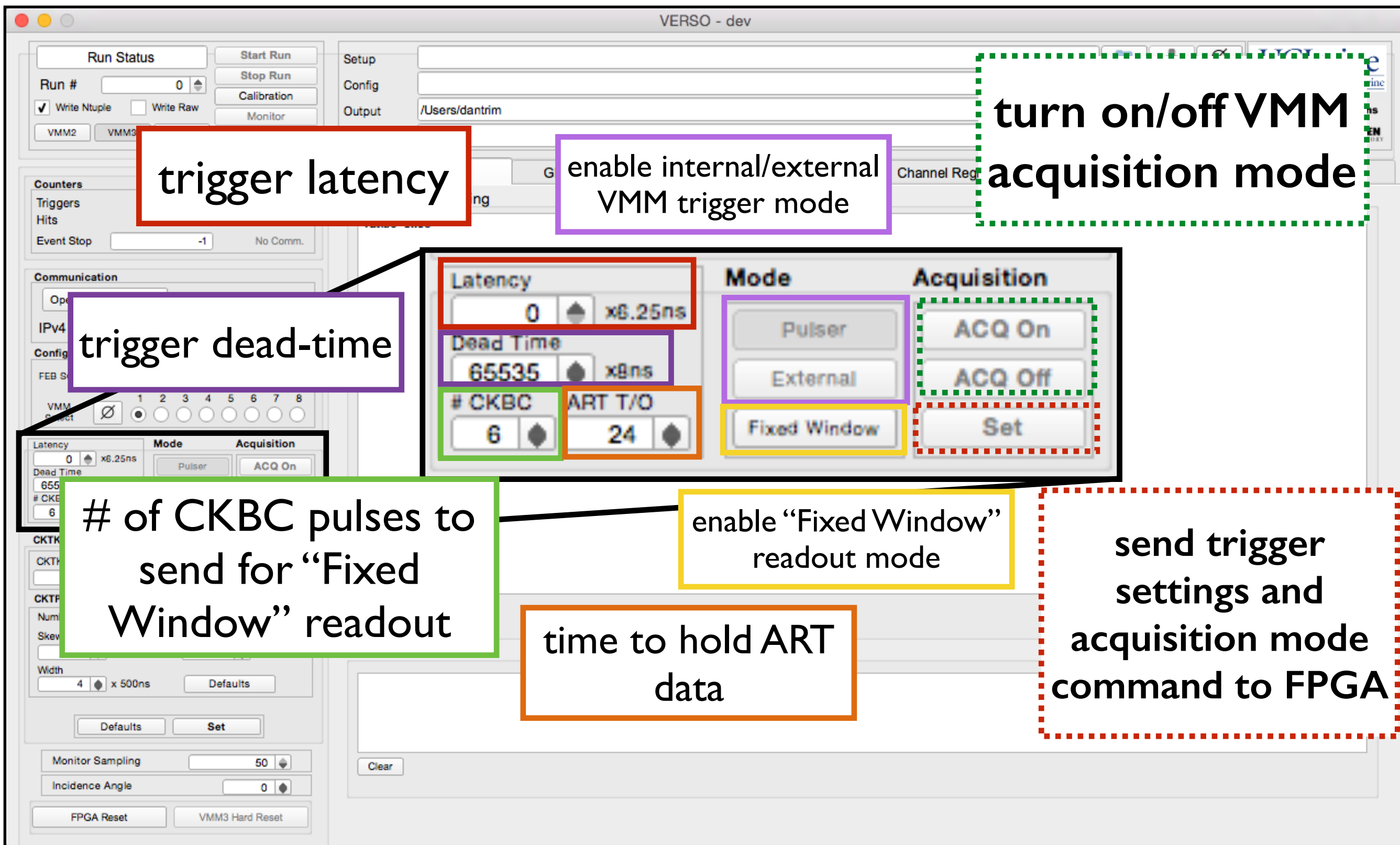


The image shows the VERSO - dev software interface with several callouts explaining key features:

- setup UDP paths and test (ping) FEB connection** (Red box)
- base IP address (address of *first* FEB)** (Green box)
- # of FEBs to talk to** (Blue box)
- FEB # to send VMM SPI to (also sets to which FEB we send all other commands)** (Purple box)
- VMM id on selected FEB to configure** (Purple box)
- send VMM SPI to selected FEB + VMMs** (Yellow box)

The interface includes sections for Counters, Messages, Global Registers, Channel Registers, Calibration, and Set IP. The Communication section is highlighted, showing fields for IPv4 (192.168.0.2) and # FEBs (1). The Configure section shows FEB Select (All) and VMM Select (1).

board and VMM selection + configuration



The screenshot shows the VERSO - dev software interface. The top section includes a 'Run Status' area with 'Run # 0', 'Write Ntuple' checked, and 'Write Raw' unchecked. Below this are 'Start Run', 'Stop Run', 'Calibration', and 'Monitor' buttons. The 'Setup' section has 'Config' and 'Output' fields. The 'Counters' section shows 'Triggers', 'Hits', and 'Event Stop'. The 'Communication' section has 'Op', 'IPv4', 'Config', and 'FEB S' fields. The 'VMM' section has a 'Select' dropdown and a row of buttons numbered 1 to 8. The 'Latency' section has a value of 0 with a multiplier of x8.25ns. The 'Dead Time' section has a value of 65535 with a multiplier of x8ns. The '# CKBC' section has a value of 6. The 'ART T/O' section has a value of 24. The 'Mode' section has buttons for 'Pulser', 'External', and 'Fixed Window'. The 'Acquisition' section has buttons for 'ACQ On', 'ACQ Off', and 'Set'. The bottom section has 'Monitor Sampling' (50), 'Incidence Angle' (0), 'FPGA Reset', and 'VMM3 Hard Reset' buttons. A 'Clear' button is also present.

turn on/off VMM acquisition mode

trigger latency

enable internal/external VMM trigger mode

trigger dead-time

of CKBC pulses to send for "Fixed Window" readout

enable "Fixed Window" readout mode

time to hold ART data

send trigger settings and acquisition mode command to FPGA

trigger settings and acquisition mode

CKTK and CKBC
configuration (40, 20, & 10
MHz CKBC possible)

CKTP (test pulse)
configuration

send fixed # of
pulses (<0 for no-
limit) (value stored
in output file)

CKTP skew w.r.t. CKBC
(1 ns steps for 40 ns clock,
6.25 ns steps otherwise)

send CKTK, CKBC, and
CKTP configuration to
the FEB

FPGA clocks configuration



The screenshot shows the VERSO - dev software interface. The interface is divided into several sections: Run Status, Setup, Counters, Communication, Configure, Latency, Mode, Acquisition, CKTK & CKBC, CKTP, and FEC Response. The Run Status section includes buttons for Start Run, Stop Run, Calibration, Monitor, and DataFlow, along with a Run # field and checkboxes for Write Ntuple and Write Raw. The Setup section includes fields for Config, Output, and Comments. The Counters section includes fields for Triggers, Hits, and Event Stop. The Communication section includes buttons for Open Communication and Establish Comms, and fields for IPv4, # FEBs, and # FEBs. The Configure section includes a FEB Select dropdown and a VMM Select dropdown. The Latency section includes fields for Latency, Dead Time, and # CKBC. The Mode section includes buttons for Pulser, External, and Fixed Window. The Acquisition section includes buttons for ACQ On, ACQ Off, and Set. The CKTK & CKBC section includes fields for CKTK Max, CKBC Freq (MHz), and Defaults. The CKTP section includes fields for Number of Pulses to Send, Skew (steps), Width, and Period. The FEC Response section includes a Clear button. The interface also features logos for UC Irvine, N.T.U. Athens, and Brookhaven National Laboratory.

event sampling rate
parameter (for sending to
vmm-mon application)

Monitor Sampling 50

Incidence Angle 0

incident angle of detector
w.r.t., e.g., beam (stored in
output files)

Monitor Sampling 50

Incidence Angle 0

FPGA Reset VMM3 Hard Reset



VERSO - dev

Run Status

Run # 0

☒ Write Ntuple ☐ Write Raw

VMM2 VMM3 L0 R/O

Start Run
Stop Run
Calibration
Monitor
DataFlow

Setup
Config
Output /Users/dantrim
Comments

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Global Registers 1
Global Registers 2
Channel Registers
Calibration
Set IP

Counters

Triggers 0
Hits 0
Event Stop -1

Communication

Open Communication Establish

IPv4 192 168 0 2 # FEBs 1

Configure

FEB Select All Configure

VMM Select 1 2 3 4 5 6 7 8

Latency 0 x6.25ns
Dead Time 65535 x8ns
CKBC ART T/O 6 24

Mode Acquisition

Pulser ACQ On
External ACQ Off
Fixed Window Set

CKTK & CKBC

CKTK Max 7 CKBC Freq. (MHz) 40 Defaults

CKTP

Number of Pulses to Send -1
Skew (steps) 0 x 1ns Period 30000 x 200ns
Width 4 x 500ns Defaults

Defaults Set

Monitor Sampling 50
Incidence Angle 0

FPGA Reset VMM3 Hard Reset

Bottom

FEC Response

Clear

Verbose

send FPGA reset command

FPGA Reset VMM3 Hard Reset

send VMM hard reset command

resets

associated bit
names in-line

VERSO - dev

trim

VMM2 VMM3 L0 R/O DataFlow Comments

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Messages Global Registers 1 Global Registers 2 Channel Registers Calibration Set IP

Global Configuration Registers

Test Pulse DAC [sdp10] 300 Ch. Polarity [sp] Negative Ch. Gain [sg] 3.0 mV/fC Peak Time [st] 200 ns

Threshold DAC [sdt10] 300 Neighbor Logic [sng] Disabled TAC Slope Adj. [stc] 60 ns Sub-hysteresis [ssh] Disabled

Leakage Curr. [slg] Enabled An. Tristates [sdrv] Disabled Dyn. Discharge [sfm] Disabled Dis. at Peak [sdp] Disabled

Monitor Multiplexing

Ch. Monitor [sm5-sm0] 0 Monitor Mode [scmx] Enabled (Channel) Route to PDO Output [sbmx] Disabled

Analog Buffer

TDO analog output [sbft] Disabled PDO analog output [sbfp] Disabled MO analog output [sbfm] Enabled

ADC Enable

6-bit mode [s6b] Disabled 8-bit mode [s8b] Enabled Hi. Res. (10-bit/8-bit) [s10b] Enabled

Direct Timing Output

Enable [sttt] Disabled Mode TtP (Thresh-to-Pk) [stpp] 0 [stot] 0

Address in Real Time (ART)

Enable ART [sfa] Disabled Detect Mode [sfam] Timing at Threshold

ADC Conversion

10-bit time [sc10b] 200 ns 8-bit time [sc8b] 100 ns 6-bit time [sc6b] Low

Dual Clocks Enable

Data [sdcks] Disabled ART [sdcka] Disabled 6-bit [sdck6b] Disabled

Counters

Triggers 0

Hits 0 Clear

Event Stop -1 No Comm.

Communication

Open Communication Establish Comms

IPv4 192 168 0 2 # FEBs 1

Configure

FEB Select All Configure

VMM Select 1 2 3 4 5 6 7 8

Latency 0 x8.25ns

Dead Time 65535 x8ns

CKBC ART T/O 6 24

Mode

Pulser ACQ On

External ACQ Off

Fixed Window Set

CKTK & CKBC

CKTK Max 7 CKBC Freq. (MHz) 10 Defaults

CKTP

Number of Pulses to Send -1

Skew (steps) 0 x 6.25ns Period 30000 x 200ns

Width 4 x 500ns Defaults

Defaults Set

Monitor Sampling 50

Incidence Angle 0

FPGA Reset VMM3 Hard Reset

VMM SPI configuration — global registers I panel

associated bit
names in-line

VERSO - dev

trim

VMM2 VMM3 L0 R/O DataFlow Comments

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Messages Global Registers 1 Global Registers 2 Channel Registers Calibration Set IP

Global Configuration Registers

Direct Out I/Os [slvs]	Disabled	ART flag sync. [ssart]	Disabled	Skip Channels 16-47 [s32]	Disabled
Tail cancellation [stlc]	Disabled	Fast recovery [srec]	Disabled	Bipolar shape [sbip]	Disabled
Auto-reset [stcr]	Disabled	Reset at 6b compl. [sfrst]	Disabled	Time ramp at thresh. [srat]	Disabled

100 Ohm SLVS Termination

On CKBC [slvsbc]	Disabled	On CKTP [slvstp]	Disabled	On CKTK [slvstk]	Disabled	On CKDT [slvsdt]	Disabled
On CKART [slvsart]	Disabled	On CKTKI [slvstki]	Disabled	On CKENA [slvsena]	Disabled	On CK6b [slvs6b]	Disabled

L0

L0 core [sL0ena]	Disabled (Reset)	Mixed signals in L0 [sL0enaV]	Disabled	L0 BC offset [l0offset] (0-4095)	4060
Ch. tagging BC offset [offset] (0-4095)	0	Ch. tagging BC rollover [rollover] (0-4095)	4095	Trig. window size [window] (0-7)	7
Max hits per L0 [truncate] (0-63)	63	# L0 to skip on overflow [nskip] (0-127)	0	Clocks w/ L0 disabled [sL0cktest]	Disabled
Invert BCCLK [sL0ckinv]	Disabled	Invert DCK [sL0dckinv]	Disabled	BCID skip [nskipm]	Disabled

Configuration Reset

Hard Reset [reset]	Disabled
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Counters

Triggers 0

Hits 0

Event Stop -1

Clear

No Comm.

Communication

Open Communication

Establish Comms

IPv4 192 168 0 2 # FEBs 1

Configure

FEB Select All

Configure

VMM Select

Latency 0 x8.25ns

Dead Time 65535 x8ns

CKBC 6 ART T/O 24

Mode

Pulser

External

Fixed Window

Acquisition

ACQ On

ACQ Off

Set

CKTK & CKBC

CKTK Max 7

CKBC Freq. (MHz) 10

Defaults

CKTP

Number of Pulses to Send -1

Skew (steps) 0 x 6.25ns

Period 30000 x 200ns

Width 4 x 500ns

Defaults

Set

Monitor Sampling 50

Incidence Angle 0

FPGA Reset

VMM3 Hard Reset

VMM SPI configuration — global registers II panel

associated bit
names in-line

VERSO - dev

trim

VMM2 VMM3 L0 R/O DataFlow Comments

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Counters
Triggers 0
Hits 0
Event Stop -1 No Comm.

Communication
Open Communication Establish Comms
IPv4 192 168 0 2 # FEBs 1

Configure
FEB Select All Configure
VMM Select 1 2 3 4 5 6 7 8

Latency 0 x8.25ns
Dead Time 65535 x8ns
CKBC 6 ART T/O 24

Mode Acquisition
Pulser ACQ On
External ACQ Off
Fixed Window Set

CKTK & CKBC
CKTK Max 7 CKBC Freq. (MHz) 10 Defaults

CKTP
Number of Pulses to Send -1
Skew (steps) 0 x 6.25ns Period 30000 x 200ns
Width 4 x 500ns Defaults
Defaults Set

Monitor Sampling 50
Incidence Angle 0
FPGA Reset VMM3 Hard Reset

Messages Global Registers 1 Global Registers 2 Channel Registers Calibration Set IP

CH	SC	SL	STH	ST	SM	0 mV	SMX	0	0	0	CH	SC	SL	STH	ST	SM	0 mV	SMX	0	0	0
0						0 mV		0	0	0	32						0 mV		0	0	0
1						0 mV		0	0	0	33						0 mV		0	0	0
2						0 mV		0	0	0	34						0 mV		0	0	0
3						0 mV		0	0	0	35						0 mV		0	0	0
4						0 mV		0	0	0	36						0 mV		0	0	0
5						0 mV		0	0	0	37						0 mV		0	0	0
6						0 mV		0	0	0	38						0 mV		0	0	0
7						0 mV		0	0	0	39						0 mV		0	0	0
8						0 mV		0	0	0	40						0 mV		0	0	0
9						0 mV		0	0	0	41						0 mV		0	0	0
10						0 mV		0	0	0	42						0 mV		0	0	0
11						0 mV		0	0	0	43						0 mV		0	0	0
12						0 mV		0	0	0	44						0 mV		0	0	0
13						0 mV		0	0	0	45						0 mV		0	0	0
14						0 mV		0	0	0	46						0 mV		0	0	0
15						0 mV		0	0	0	47						0 mV		0	0	0
16						0 mV		0	0	0	48						0 mV		0	0	0
17						0 mV		0	0	0	49						0 mV		0	0	0
18						0 mV		0	0	0	50						0 mV		0	0	0
19						0 mV		0	0	0	51						0 mV		0	0	0
20						0 mV		0	0	0	52						0 mV		0	0	0
21						0 mV		0	0	0	53						0 mV		0	0	0
22						0 mV		0	0	0	54						0 mV		0	0	0
23						0 mV		0	0	0	55						0 mV		0	0	0
24						0 mV		0	0	0	56						0 mV		0	0	0
25						0 mV		0	0	0	57						0 mV		0	0	0
26						0 mV		0	0	0	58						0 mV		0	0	0
27						0 mV		0	0	0	59						0 mV		0	0	0
28						0 mV		0	0	0	60						0 mV		0	0	0
29						0 mV		0	0	0	61						0 mV		0	0	0
30						0 mV		0	0	0	62						0 mV		0	0	0
31						0 mV		0	0	0	63						0 mV		0	0	0

VMM SPI configuration — channel registers panel

Run Status

Run #

0

☒ Write Ntuple
 ☐ Write Raw

VMM2

VMM3

L0 R/O

Start Run

Stop Run

Calibration

Monitor

DataFlow

Setup

Config

Output

Comments

Messages

Global Registers 1

Global Registers 2

Channel Registers

Calibration

Set IP

Counters

Triggers

0

Hits

0

Event Stop

-1

Clear

No Comm.

Communication

Open Communication

Establish Comms

IPv4

192

168

0

2

FEBs

1

Configure

FEB Select

All

Configure

VMM Select

1

2

3

4

5

6

7

8

Latency

0

x8.25ns

Dead Time

65535

x8ns

CKBC

6

ART T/O

24

Mode

Pulser

External

Fixed Window

ACQ On

ACQ Off

Set

CKTK & CKBC

CKTK Max

7

CKBC Freq. (MHz)

10

Defaults

CKTP

Number of Pulses to Send

-1

Skew (steps)

0

x 6.25ns

Period

30000

x 200ns

Width

4

x 500ns

Defaults

Set

Monitor Sampling

50

Incidence Angle

0

FPGA Reset

VMM3 Hard Reset

Load Calibration

Thresholds

Calibration Scan

Calibration Type

xADC

Non-xADC

Object Selection

Boards

1

VMMs

1

2

3

4

5

6

7

8

Channels

Start

0

End

63

Samples

1000

xADC Calibration

Type

☐ Threshold DAC
 ☐ Test Pulse DAC
 ☒ Channel Trims
 ☐ Baselines

Loop

Trim Step Range

Start

0

End

31

Step

1

Threshold DAC

Start

300

End

300

Step

50

Test Pulse DAC

Start

300

End

300

Step

50

Sampling Period

10000

(in 5ns steps)

Manual xADC Configuration

Calibration

Type

☒ Custom Loop
 ☐ Baselines (E)
 ☐ Baselines (N)
 ☐ Time
 ☐ Efficiency (Th.)
 ☐ Efficiency (Amp.)

Loop

Gain (mV/fC)

Start

3.0

End

3.0

Peak Time (ns)

Start

200

End

200

TAC slope (ns)

Start

60

End

60

TP Skew x 6.25ns

Start

5

End

5

Step

1

BC Lat Step x 6.25 ns

Start

0

End

0

Step

1

Threshold DAC

Start

230

End

230

Step

1

Test Pulse DAC

Start

300

End

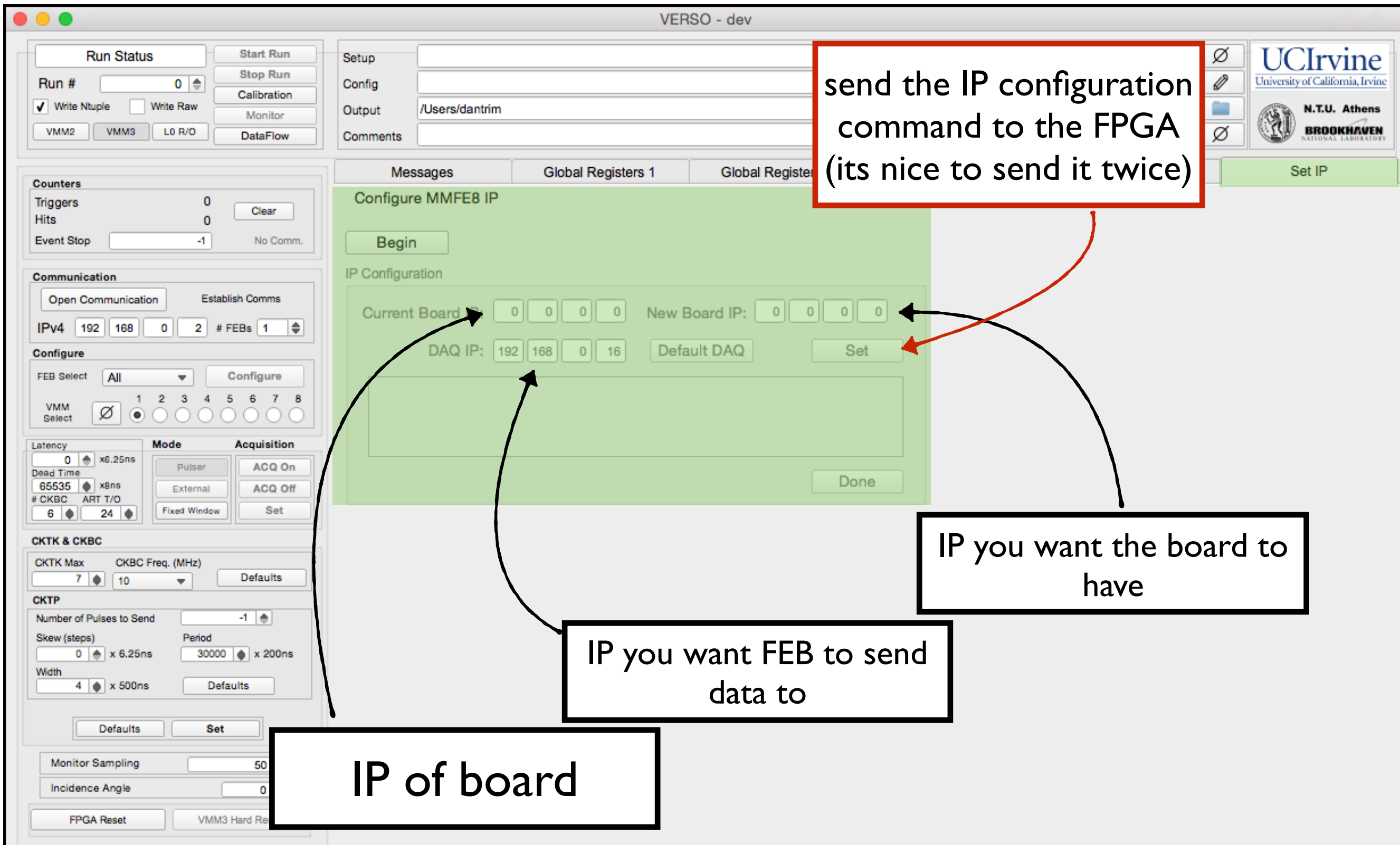
305

Step

1

☐ Chan Loop
 ☒ Chan Masking

calibration loop configuration panel



The screenshot displays the VERSO - dev software interface. The central panel is titled "Configure MMFE8 IP" and contains the "IP Configuration" section. This section includes fields for "Current Board IP" (0 0 0 0), "New Board IP" (0 0 0 0), "DAQ IP" (192 168 0 16), and a "Default DAQ" button. A "Set" button is also present. A red box highlights the "Set IP" button in the top right corner, with a red arrow pointing to it and a text box stating "send the IP configuration command to the FPGA (its nice to send it twice)". A black arrow points from the "Set IP" button to the "New Board IP" field, with a text box stating "IP you want the board to have". Another black arrow points from the "Set IP" button to the "DAQ IP" field, with a text box stating "IP you want FEB to send data to". A third black arrow points from the "Set IP" button to the "Current Board IP" field, with a text box stating "IP of board". The interface also includes a "Run Status" section on the left with buttons for "Start Run", "Stop Run", "Calibration", "Monitor", and "DataFlow". The "Communication" section on the left has buttons for "Open Communication" and "Establish Comms". The "Configure" section on the left has a "FEB Select" dropdown and a "Configure" button. The "Latency" section on the left has a "Dead Time" field and a "Set" button. The "CKTK & CKBC" section on the left has a "CKTK Max" field and a "Set" button. The "CKTP" section on the left has a "Number of Pulses to Send" field and a "Set" button. The "Monitor Sampling" section on the left has a "Monitor Sampling" field and a "Set" button. The "Incidence Angle" section on the left has an "Incidence Angle" field and a "Set" button. The "FPGA Reset" button is at the bottom left. The "VMM3 Hard Re" button is at the bottom right. The "Messages" tab is selected in the top right. The "Global Registers 1" and "Global Register" tabs are also visible. The "UC Irvine" logo is in the top right corner. The "N.T.U. Athens" and "BROOKHAVEN NATIONAL LABORATORY" logos are also visible. The "Set IP" button is highlighted in green.

Run Status

Run # 0

Write Ntuple Write Raw

VMM2 VMM3 L0 R/O

Start Run Stop Run Calibration Monitor DataFlow

Setup Config Output /Users/dantrim Comments

Messages Global Registers 1 Global Register

Configure MMFE8 IP

Begin

IP Configuration

Current Board IP: 0 0 0 0 New Board IP: 0 0 0 0

DAQ IP: 192 168 0 16 Default DAQ Set

Done

send the IP configuration command to the FPGA (its nice to send it twice)

IP you want the board to have

IP you want FEB to send data to

IP of board

Set IP

FEB IP configuration panel

Loading of the calibration loops is done within the VERSO calibration panel. When set, the next run will process these loops and build the calibration n-tuple.

Messages

Global Registers 1

Global Registers 2

Channel Registers

Calibration

Set IP

Load Calibration

Thresholds

Calibration Scan

Calibration Type

xADC

Non-xADC

Object Selection

Boards

1

VMMs

1

2

3

4

5

6

7

8

Channels

Start

0

End

63

Samples

1000

xADC Calibration

Type

☐ Threshold DAC

☐ Test Pulse DAC

☒ Channel Trims

☐ Baselines

Loop

Trim Step Range	Start	<div>0</div>	End	<div>31</div>	Step	<div>1</div>
Threshold DAC	Start	<div>300</div>	End	<div>300</div>	Step	<div>50</div>
Test Pulse DAC	Start	<div>300</div>	End	<div>300</div>	Step	<div>50</div>

Sampling Period

10000

(in 5ns steps)

Manual xADC Configuration

Calibration

Type

☒ Custom Loop

☐ Baselines (E)

☐ Baselines (N)

☐ Time

☐ Efficiency (Th.)

☐ Efficiency (Amp.)

Loop

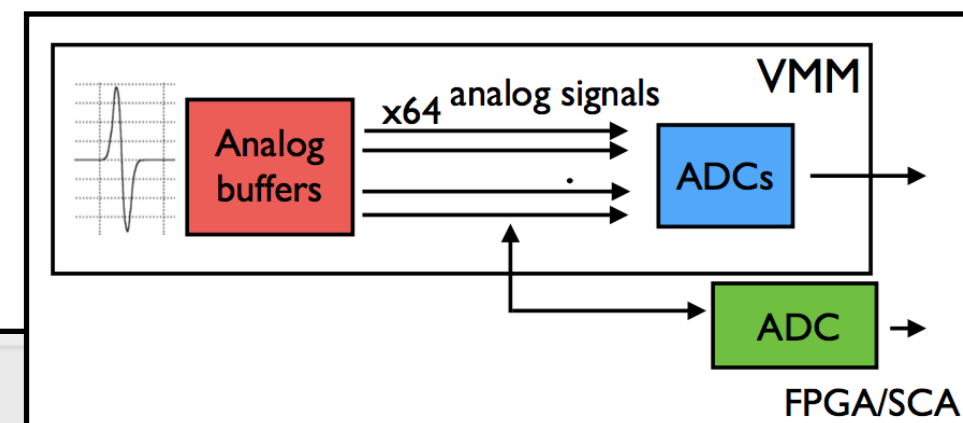
Gain (mV/fC)	Start	<div>3.0</div>	End	<div>3.0</div>	
Peak Time (ns)	Start	<div>200</div>	End	<div>200</div>	
TAC slope (ns)	Start	<div>60</div>	End	<div>60</div>	
TP Skew x 2ns	Start	<div>5</div>	End	<div>5</div>	Step <div>1</div>
BC Lat Step x 6.25 ns	Start	<div>0</div>	End	<div>0</div>	Step <div>1</div>
Threshold DAC	Start	<div>230</div>	End	<div>230</div>	Step <div>1</div>
Test Pulse DAC	Start	<div>300</div>	End	<div>305</div>	Step <div>1</div>

☐ Chan Loop

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xADC based sampling

For selected (board, chips, channels)...



Calibration Type

☒ xADC ☐ Non-xADC

Object Selection

Boards VMMs Channels Start End # Samples

xADC Calibration

Type

☐ Threshold DAC

☐ Test Pulse DAC

☒ Channel Trims

☐ Baselines

Loop

Trim Step Range	Start	End	Step
Trim Step Range	<input type="text" value="0"/>	<input type="text" value="31"/>	<input type="text" value="1"/>
Threshold DAC	<input type="text" value="300"/>	<input type="text" value="300"/>	<input type="text" value="50"/>
Test Pulse DAC	<input type="text" value="300"/>	<input type="text" value="300"/>	<input type="text" value="50"/>

Sampling Period

(in 5ns steps)

Manual xADC Configuration

samples to acquire per step

xADC sampling rate

We can perform calibration routines to sample:

1. Analog DAC levels (threshold and pulser)
2. Channel-by-channel threshold variations, stepping over the VMM threshold trimmer values
3. Channel baseline & noise levels

Output data is not standard VMM events but xADC samples

... + combinations of them

Pulser based sampling

For selected (board, chips, channels)...

Calibration

Type

- ☒ Custom Loop
- ☐ Baselines (E)
- ☐ Baselines (N)
- ☐ Time
- ☐ Efficiency (Th.)
- ☐ Efficiency (Amp.)

Loop

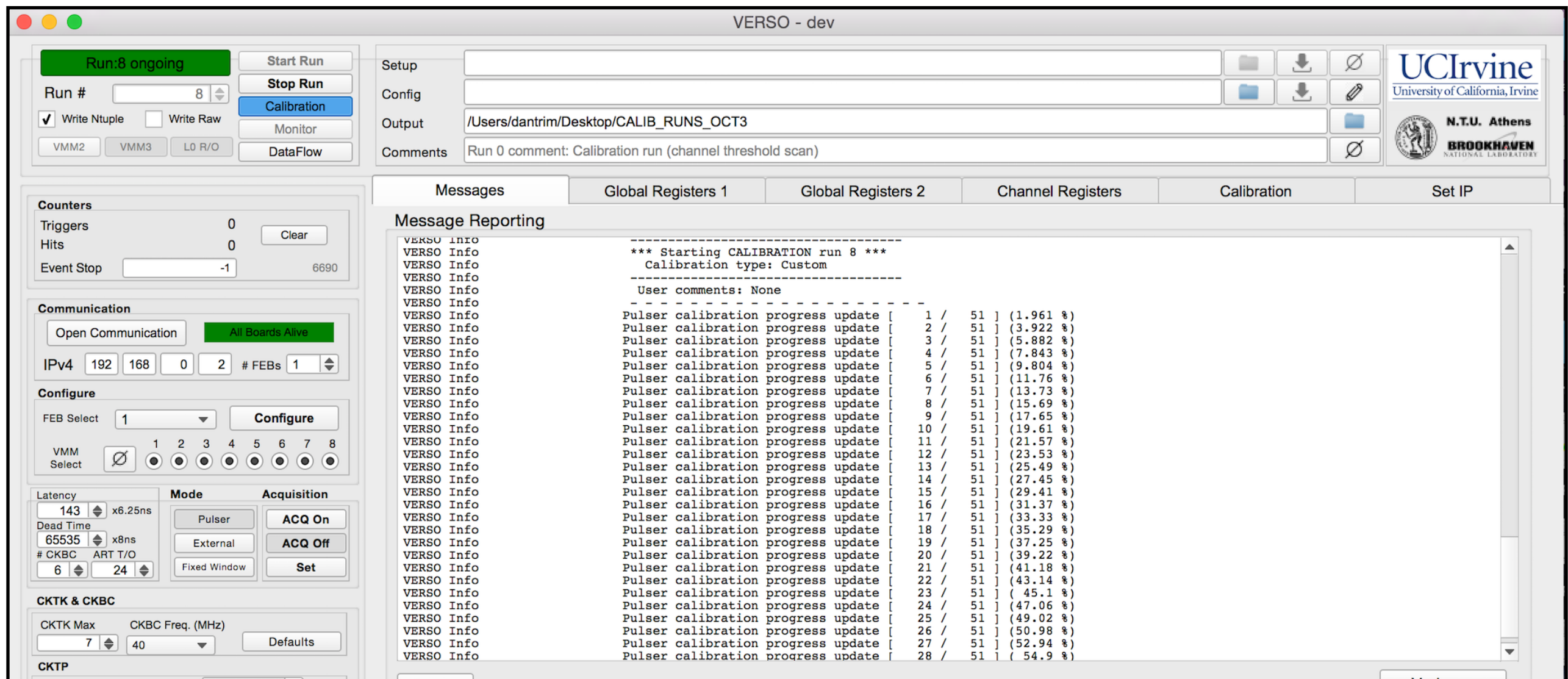
Gain (mV/fC)	Start	3.0	End	3.0	
Peak Time (ns)	Start	200	End	200	
TAC slope (ns)	Start	60	End	60	
TP Skew x 2ns	Start	5	End	5	Step 1
BC Lat Step x6.25 ns	Start	0	End	0	Step 1
Threshold DAC	Start	230	End	230	Step 1
Test Pulse DAC	Start	300	End	305	Step 1

☐ Chan Loop
☒ Chan Masking

We can perform loops over the shown parameters. The quantity will be looped over if $\text{End} \neq \text{Start}$

Output from FEB is same format as VMM event data (we are using the internal pulser) but stored slightly differently for calibration analysis purposes

- For the test beam data taking and analysis we exercised much of the calibration
 - In the time leading up to the TB, the pulser-based calibration was totally overhauled
 - Pulser-based calibration module much more robust and efficient (smarter than previous handling)

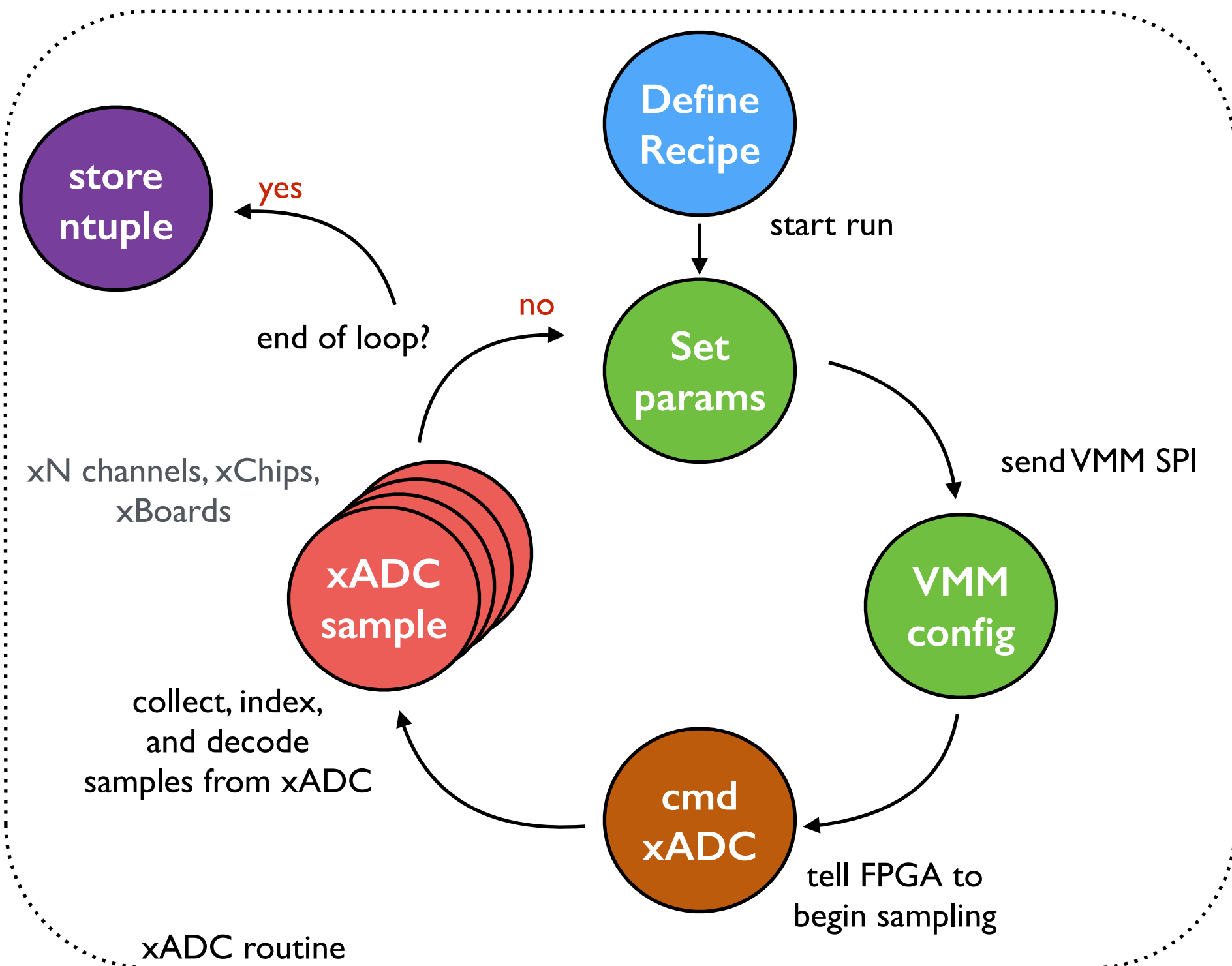


The screenshot displays the VERSO - dev software interface, which is used for configuring and monitoring the calibration process. The interface is divided into several sections:

- Run Control:** Includes a green status bar indicating "Run:8 ongoing". Below it, there are fields for "Run #" (set to 8) and buttons for "Start Run", "Stop Run", "Calibration", "Monitor", and "DataFlow". There are also checkboxes for "Write Ntuple" and "Write Raw", and buttons for "VMM2", "VMM3", and "LO R/O".
- Setup and Configuration:** A section with input fields for "Setup", "Config", and "Output" (set to "/Users/dantrim/Desktop/CALIB_RUNS_OCT3"). A "Comments" field contains the text "Run 0 comment: Calibration run (channel threshold scan)".
- Counters:** A section showing "Triggers" (0), "Hits" (0), and "Event Stop" (-1). A "Clear" button is present.
- Communication:** A section with an "Open Communication" button and a green status bar indicating "All Boards Alive". It also shows "IPv4" address (192.168.0.2) and "# FEBs" (1).
- Configure:** A section with a "FEB Select" dropdown (set to 1) and a "Configure" button. Below it, there are "VMM Select" buttons (1-8) and "Latency" (143 x6.25ns) and "Dead Time" (65535 x8ns) settings.
- Mode and Acquisition:** A section with "Mode" buttons (Pulser, External, Fixed Window) and "Acquisition" buttons (ACQ On, ACQ Off, Set).
- CKTK & CKBC:** A section with "CKTK Max" (7) and "CKBC Freq. (MHz)" (40) settings, along with a "Defaults" button.
- Message Reporting:** A large text area showing the progress of the calibration run. It starts with "*** Starting CALIBRATION run 8 ***" and "Calibration type: Custom". It then lists "User comments: None" and a series of "Pulser calibration progress update" messages for each of the 28 channels, showing the current value and percentage of completion.

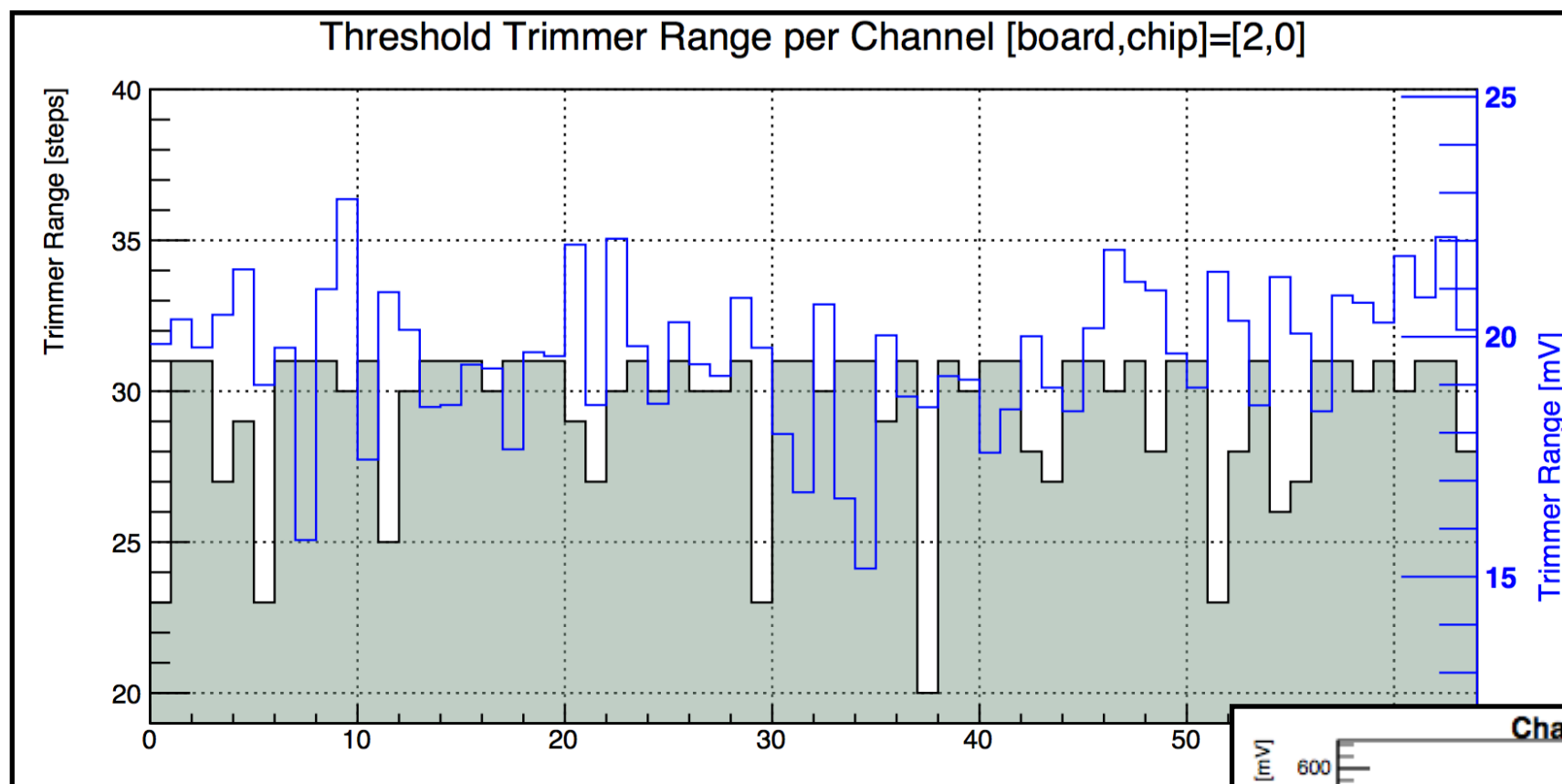
Channel Threshold Equalization

- Before initial data taking, we performed the channel threshold trimmer calibration in order to equalize the channel-by-channel response
- This is an xADC based sampling procedure that steps through the channel trimmer settings for each channel and measures the threshold with N samplings per setting

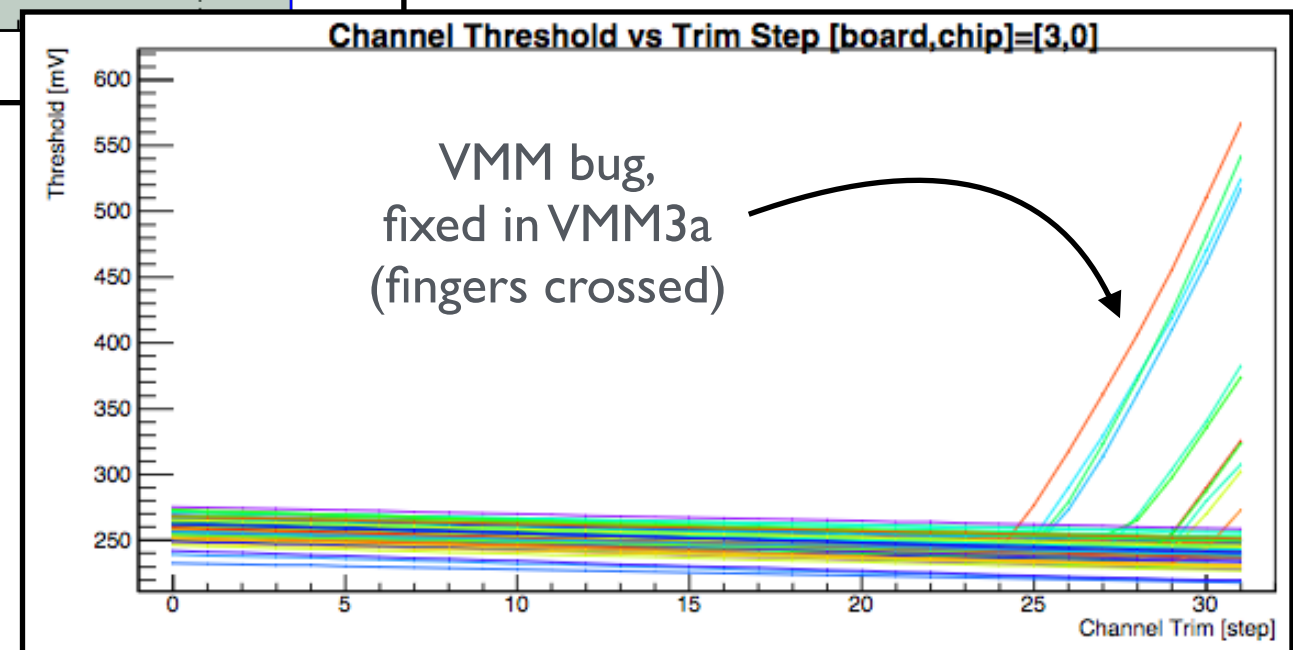


CH	SC	SL	STH	ST	SM	4 mV ▾	SMX
0						4 mV ▾	
1						4 mV ▾	
2						4 mV ▾	
3						4 mV ▾	
4						4 mV ▾	
5						4 mV ▾	
6						4 mV ▾	
7						4 mV ▾	
8						4 mV ▾	
9						4 mV ▾	
10						4 mV ▾	
11						4 mV ▾	
12						4 mV ▾	
13						4 mV ▾	
14						4 mV ▾	
15						4 mV ▾	
16						4 mV ▾	
17						4 mV ▾	
18						4 mV ▾	
19						4 mV ▾	
20						4 mV ▾	
21						4 mV ▾	
22						4 mV ▾	
23						4 mV ▾	
24						4 mV ▾	
25						4 mV ▾	
26						4 mV ▾	
27						4 mV ▾	
28						4 mV ▾	
29						4 mV ▾	
30						4 mV ▾	
31						4 mV ▾	

As we step through the trimmers, we vary each channel's threshold and get a measure of the overall channel trim range

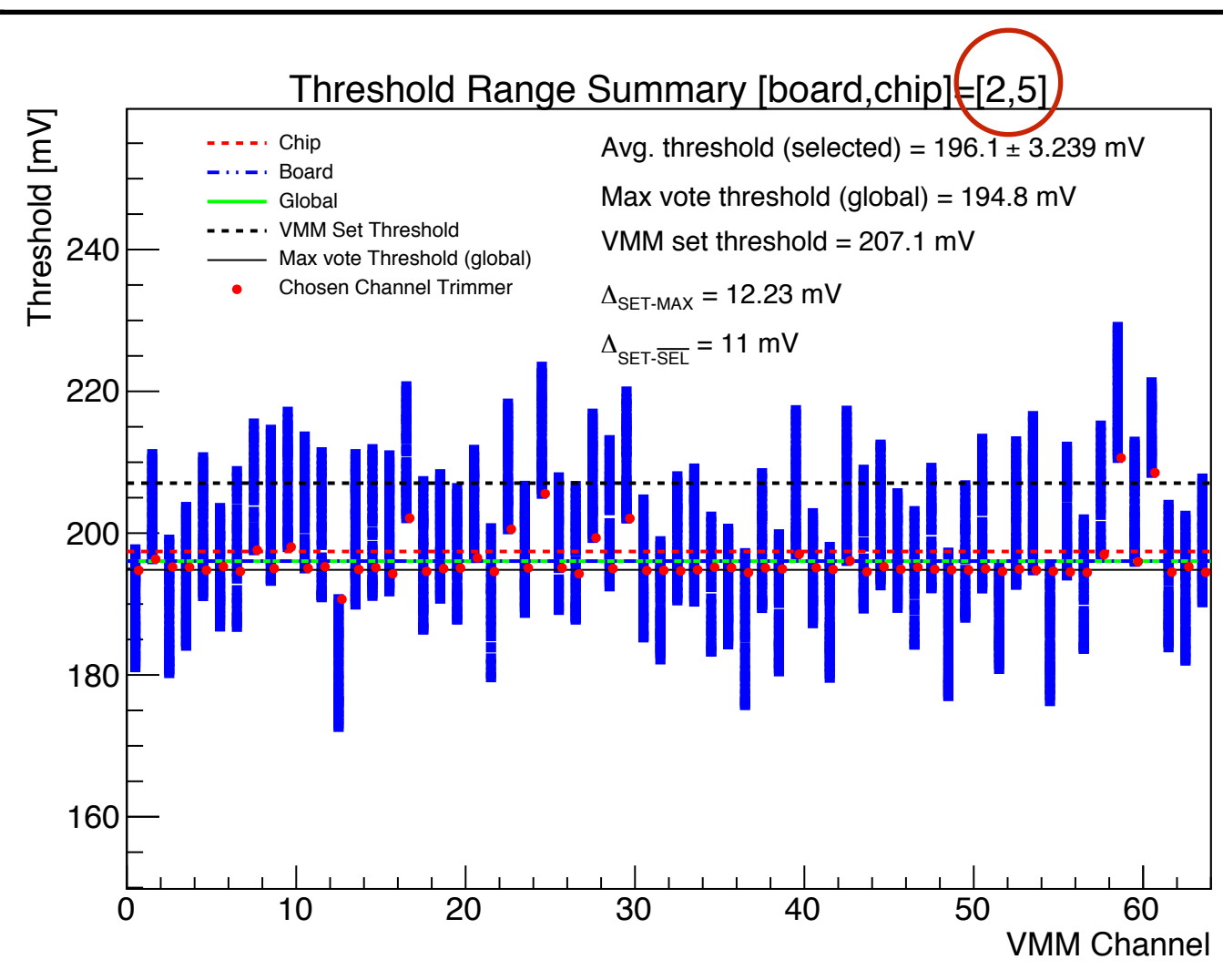
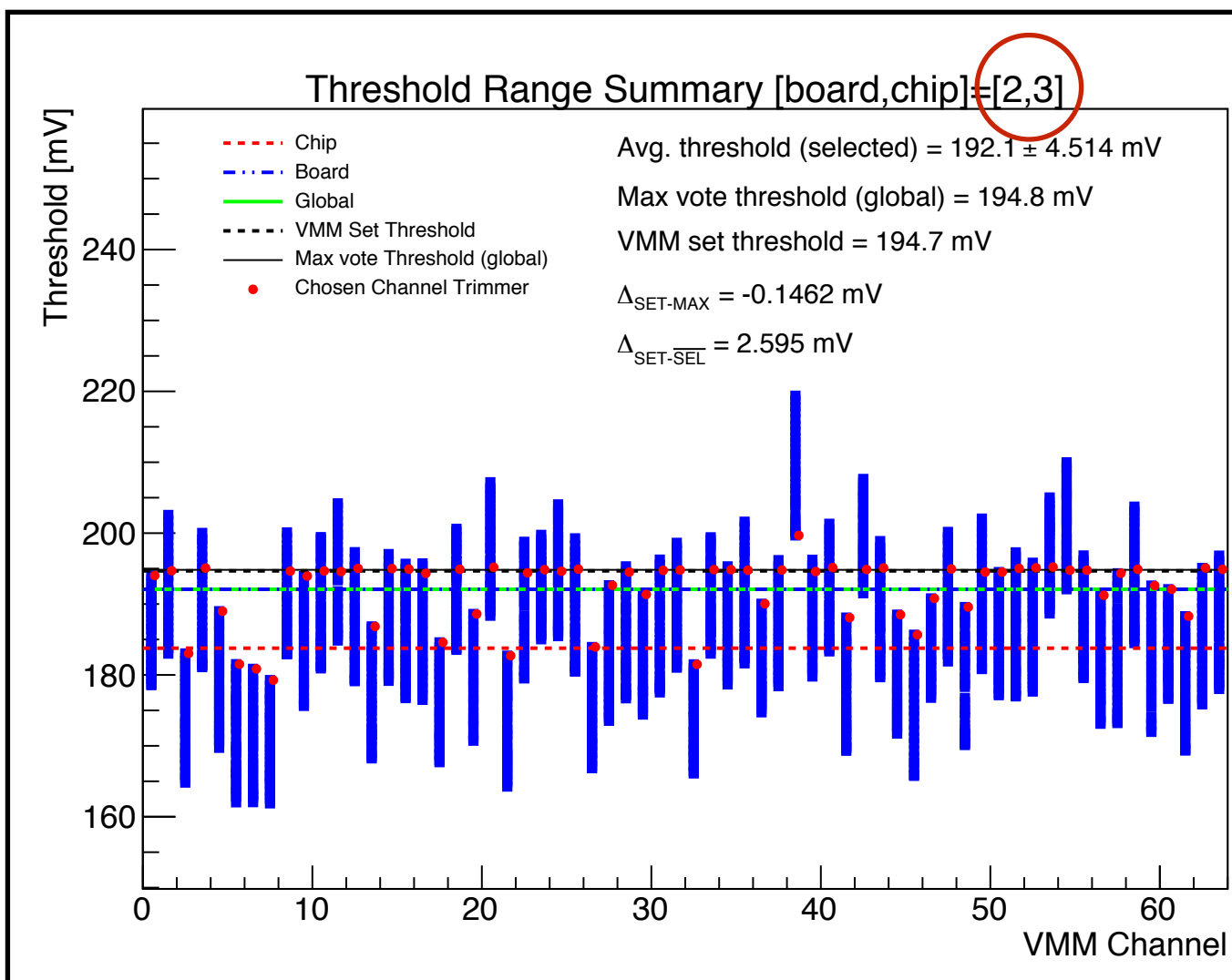


Inaccessible trim steps are detected by the calibration analysis software and not considered during the equalization procedure



The channel-by-channel threshold variation is “equalized” by a max voting procedure:

1. For all loaded boards, chips, channels, determine the threshold (mV) ranges accessible
2. Find the threshold (mV) that is attainable by the maximum number of VMM channels
3. For each VMM channel, find the trimmer setting that gets that channel closest to that “max-voted” threshold
4. Store these trimmer settings (at per chip, per board, and “global” granularity)



Channel Threshold Equalization

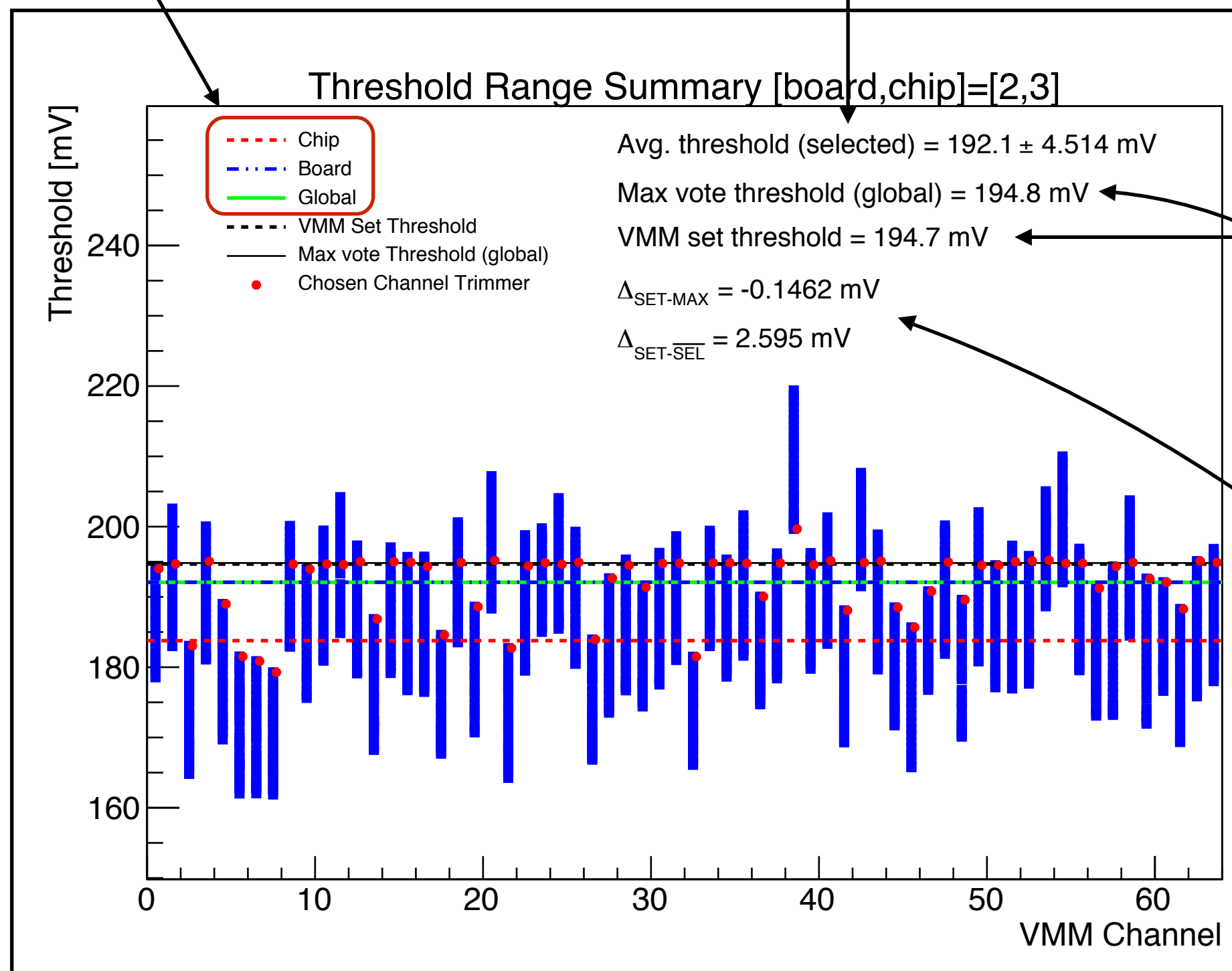


27

average thresholds at the trimmer settings that equalize at the per chip, per FEB, and “global” level

average of the threshold values at the chosen trimmers

channel trimmer calibration can load in the DAC calibration to determine the VMM threshold in mV — this VMM had threshold DAC of 230 counts



max voted threshold to every channel aspires to

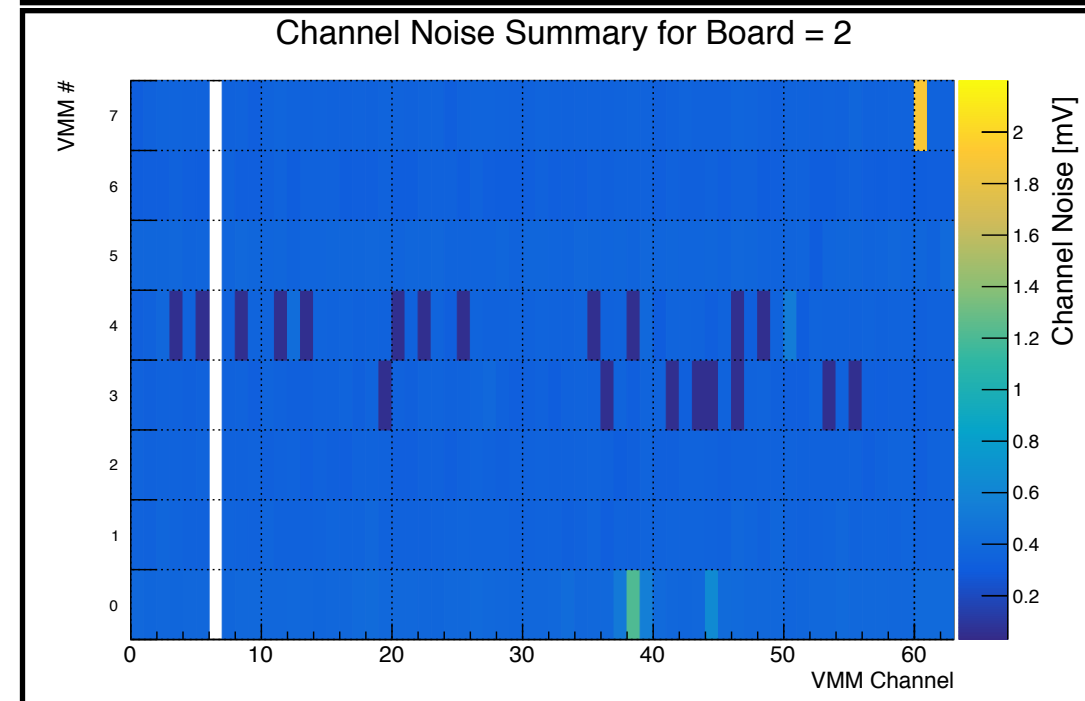
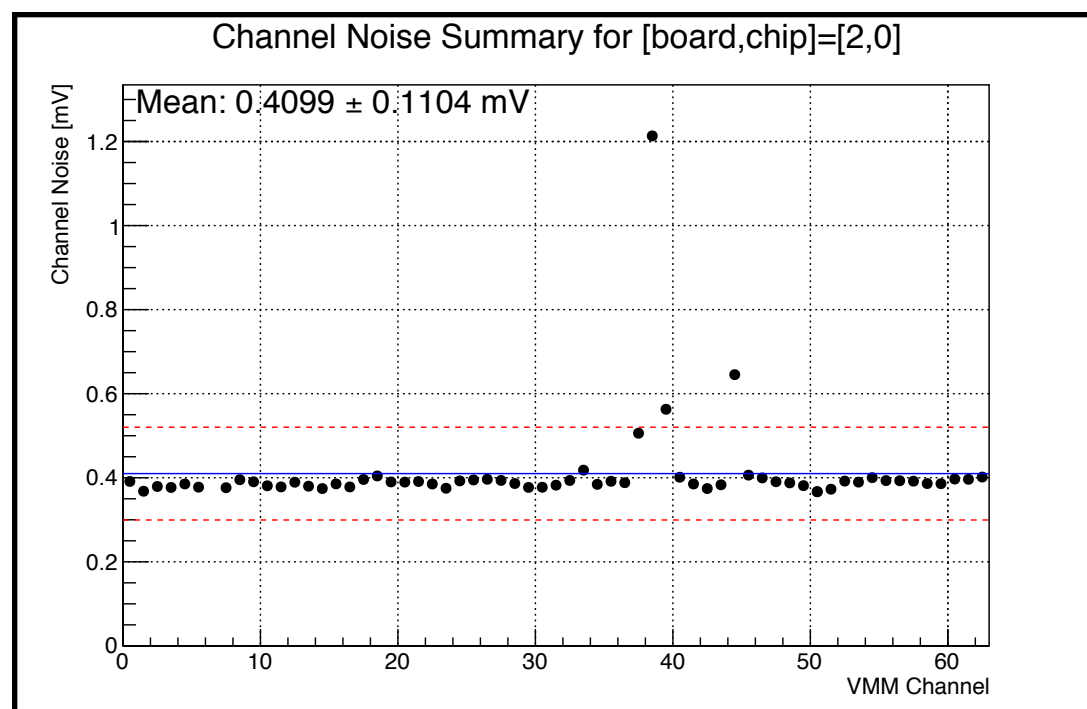
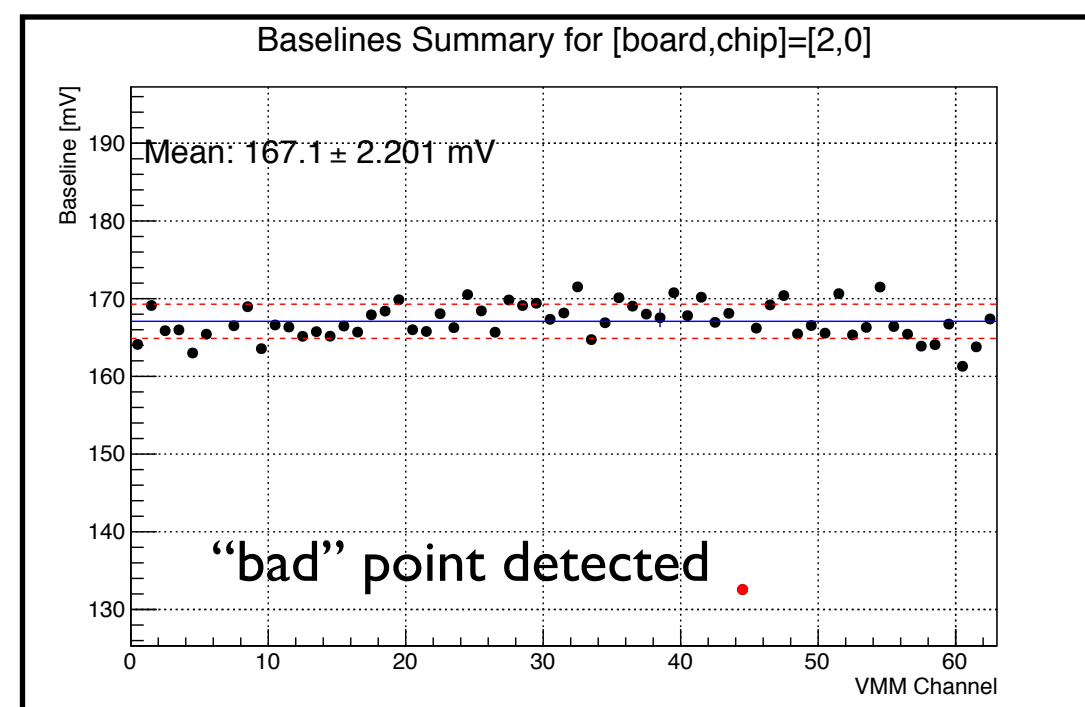
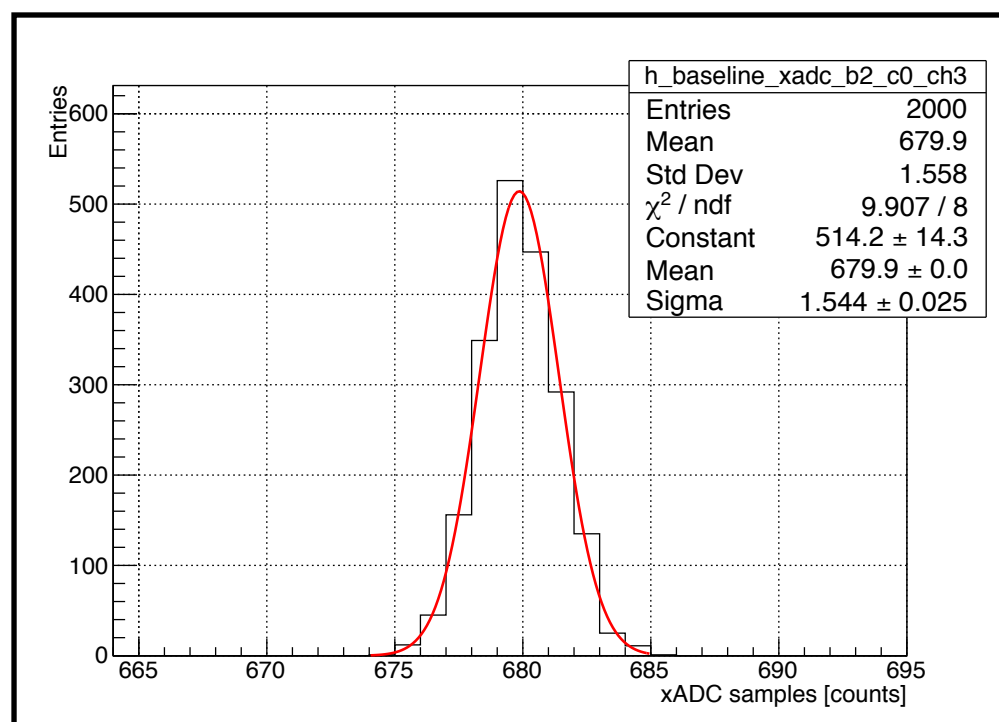
Δ 's between VMM configured threshold (DAC) and the max-voted and average-of-selected thresholds

divergent trims removed prior to all equalization

Use the xADC to sample the channel input baselines and noise

Procedure:

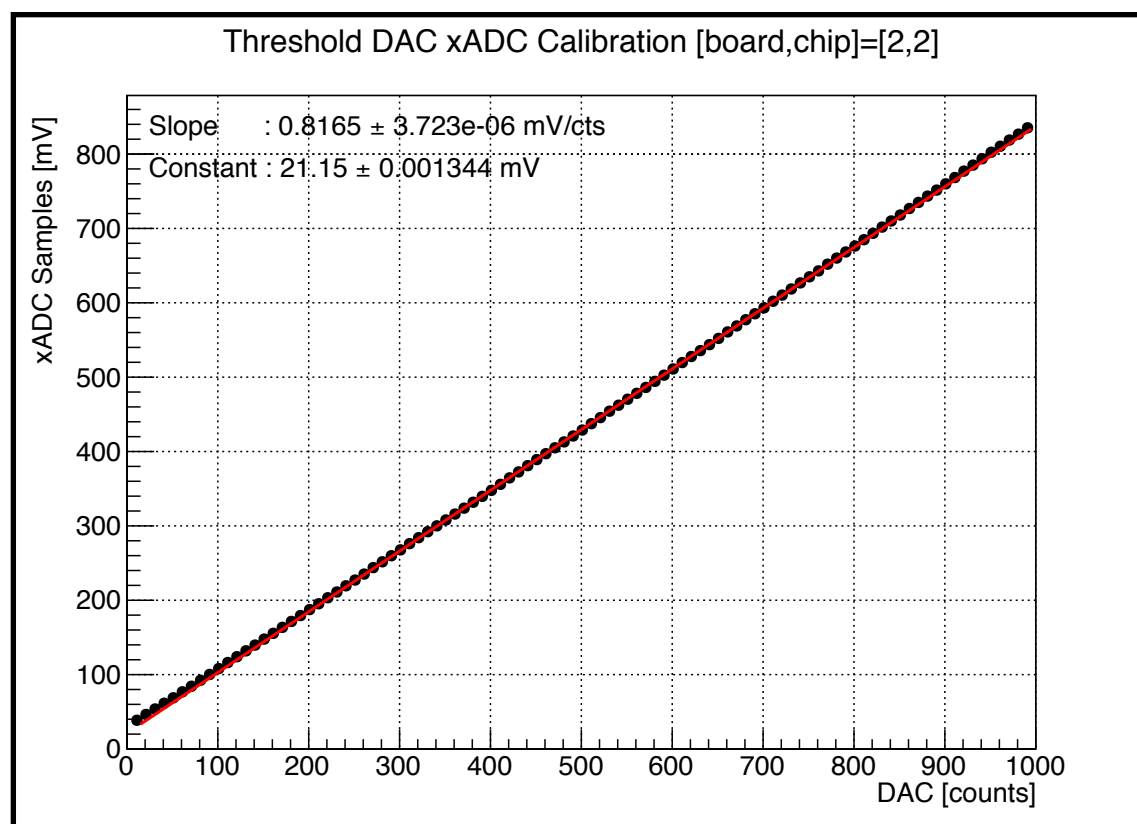
1. For each board and chip, sample each channel's input level with the xADC
2. Perform a gaussian fit of the samples per channel: mean is taken as that channel's baseline, width is taken as the channel noise



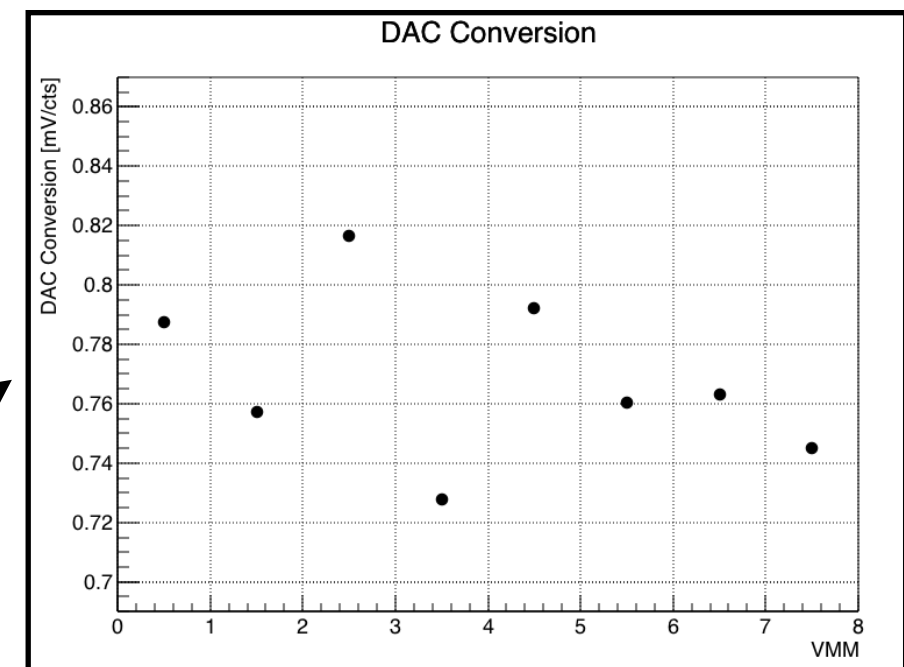
Use the xADC to sample the DAC levels

Procedure:

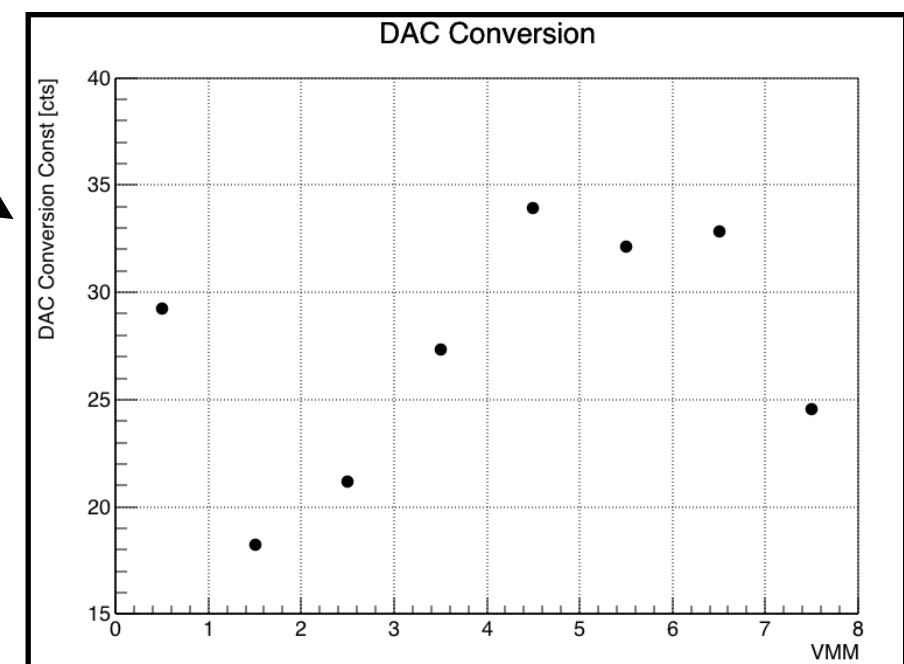
1. Step through the VMM DAC values (pulser and/or threshold)
2. At each DAC, sample the DAC levels with the xADC
3. From fit, determine conversion constants to absolute scale



slopes

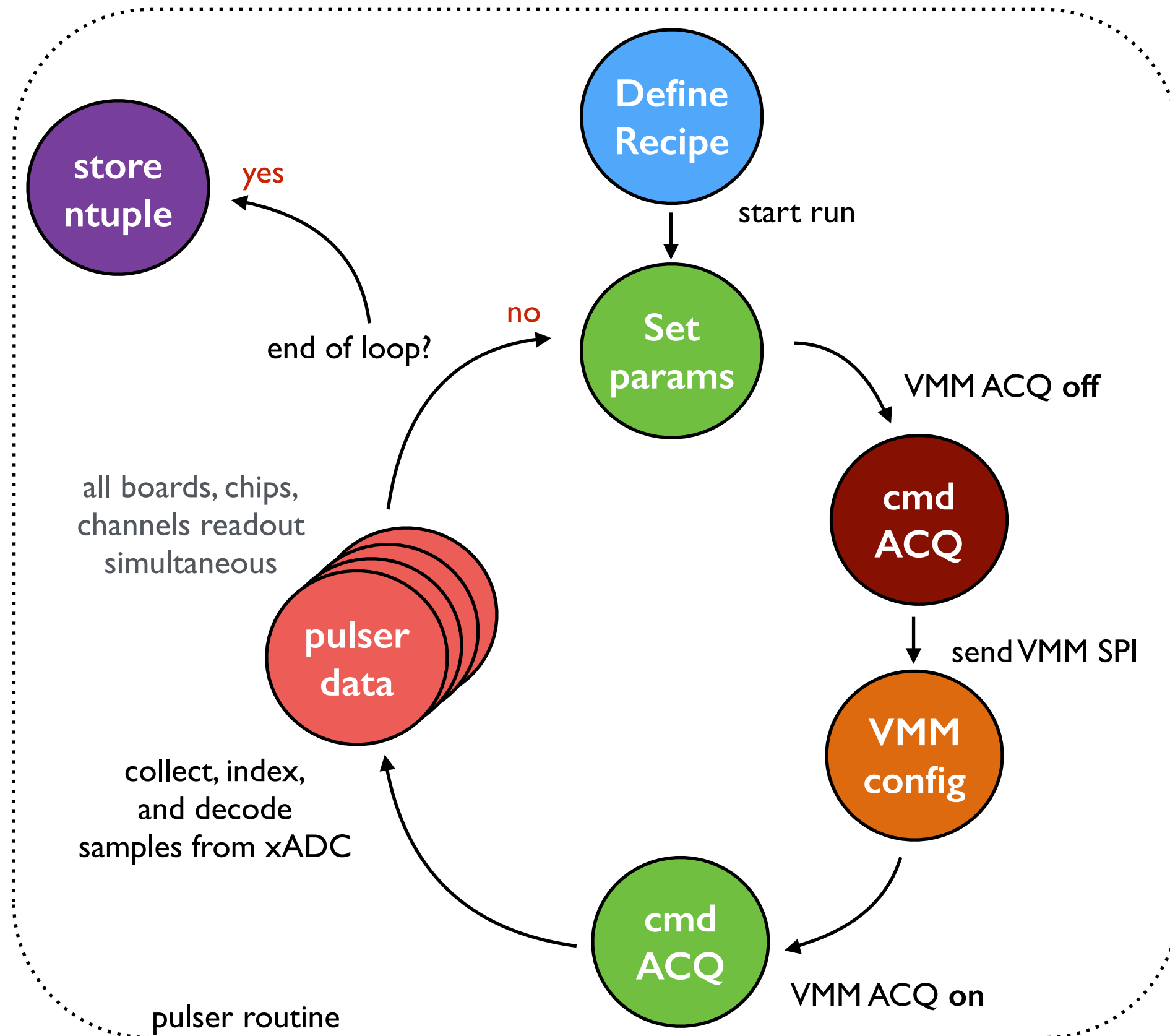


intercepts



Can load these data into to other calibration procedures and analysis

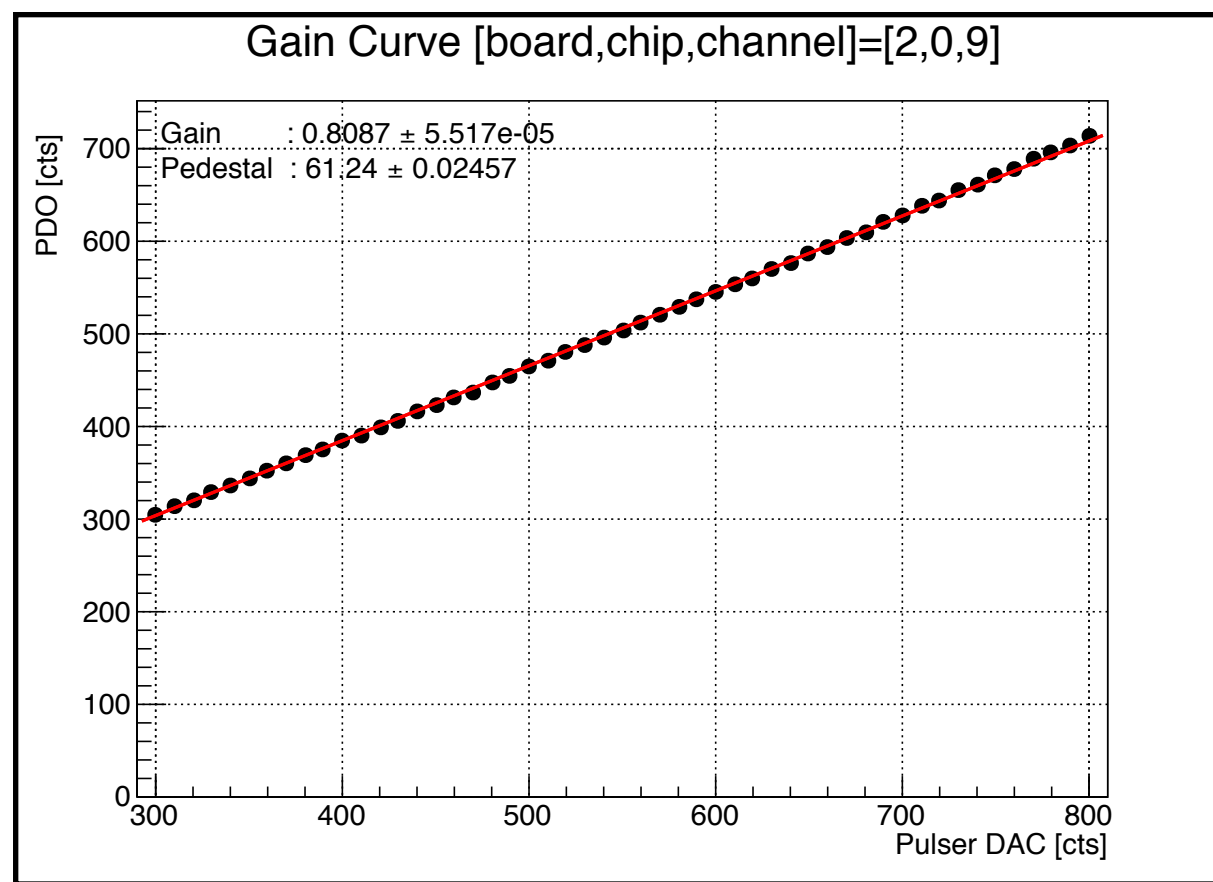
Pulser-based calibration to measure channel-by-channel variation in gain and PDO pedestal



Pulser-based calibration to measure channel-by-channel variation in gain and PDO pedestal for offline correction of the data

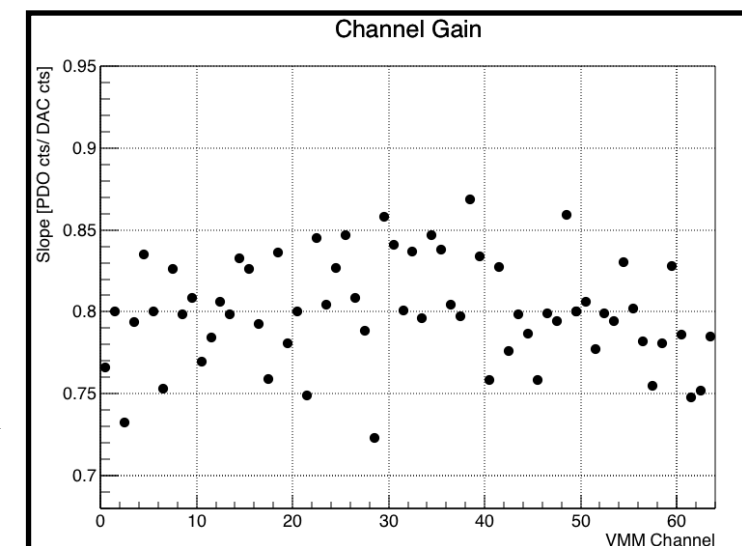
Procedure:

1. Step through pulser DAC values
2. At each DAC collect N samples per channel
3. From linear relation between PDO and DAC, get gain curve and pedestal parameters

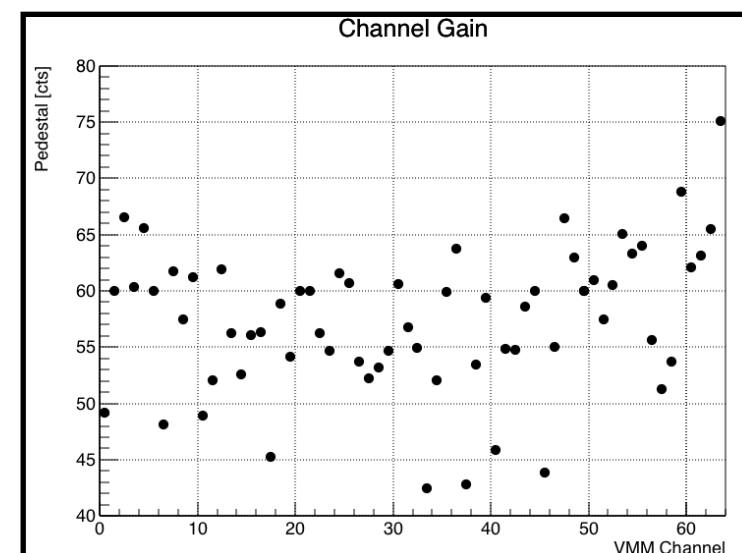


Loading the pulser DAC calibration allows you to get absolute gain in mV/fC

slopes
(gains)



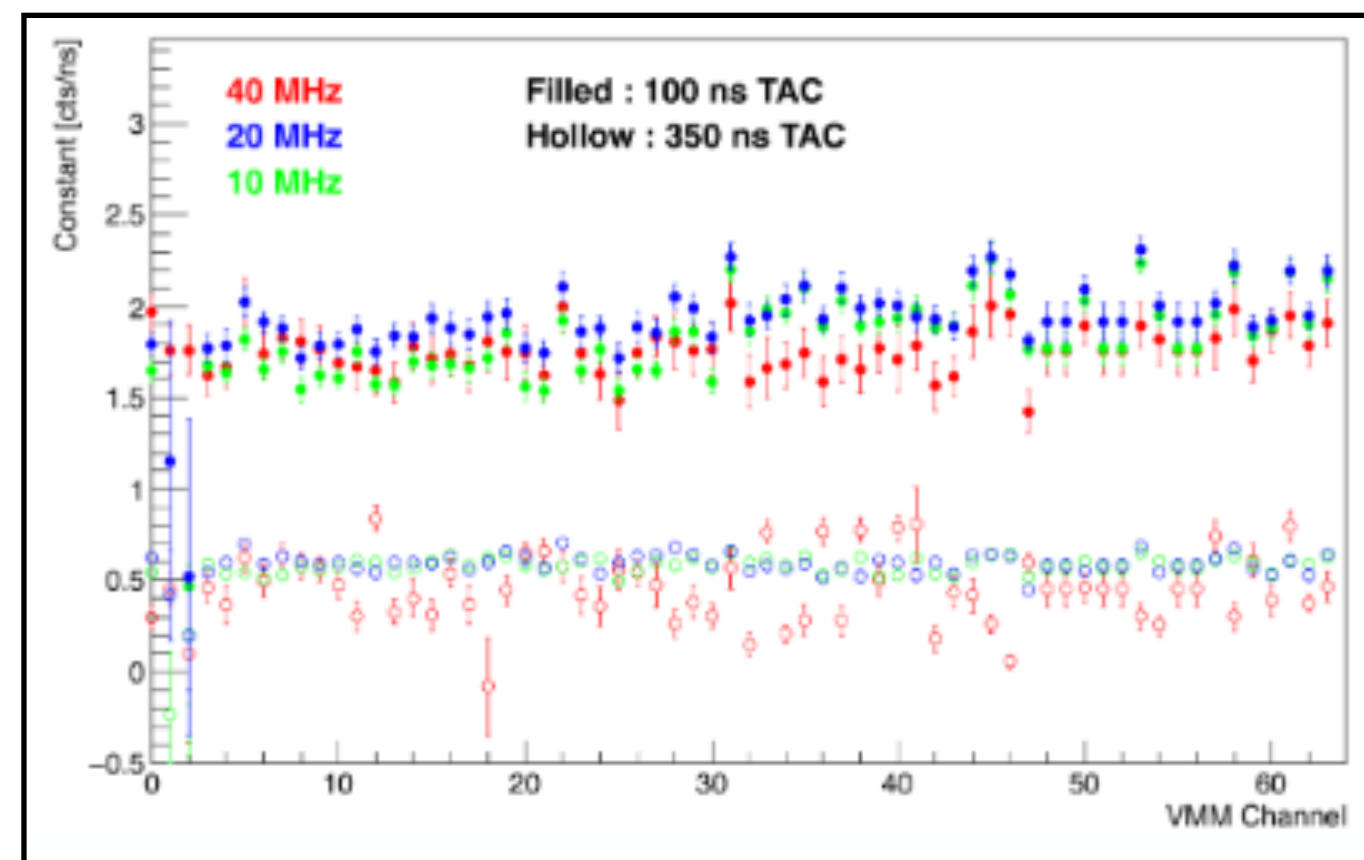
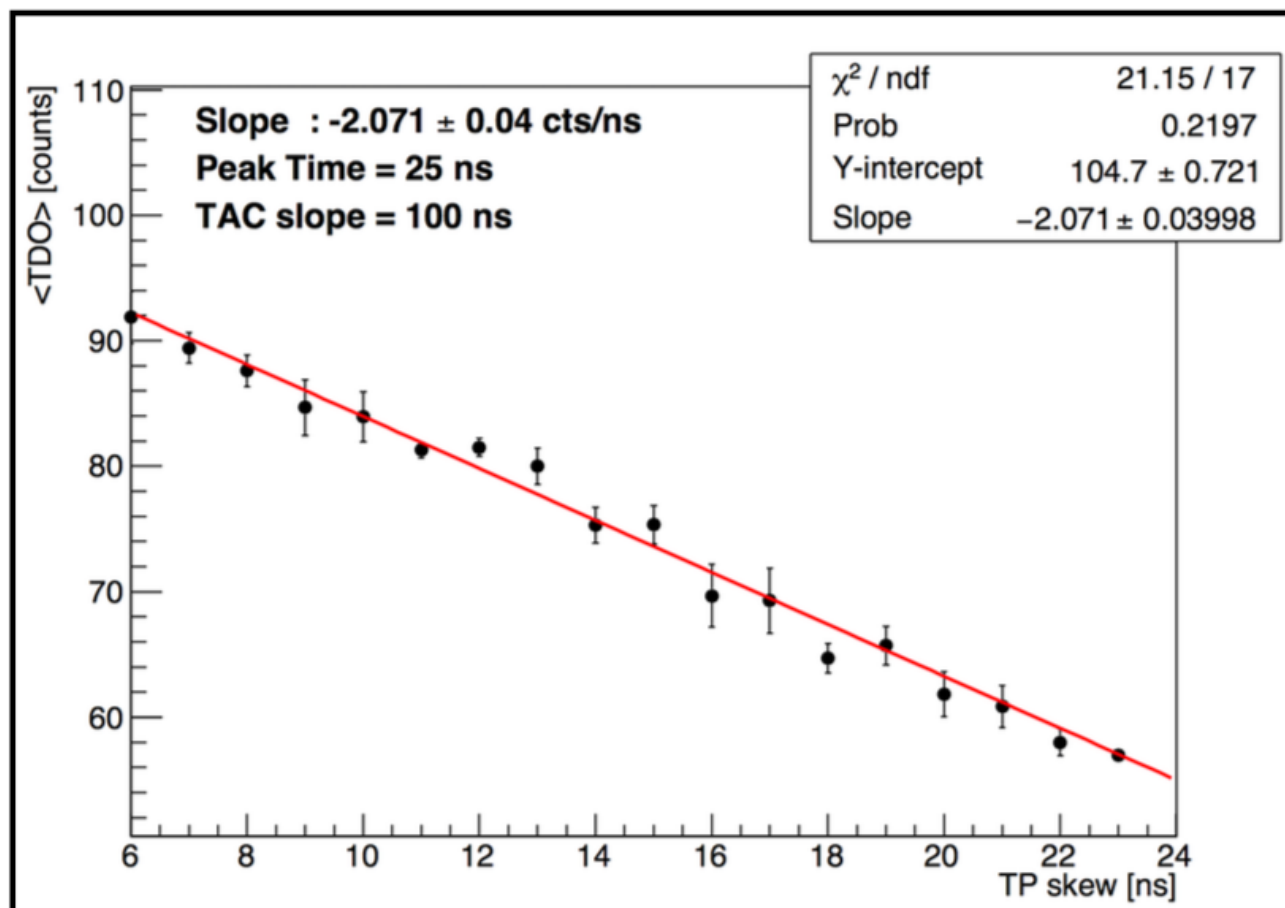
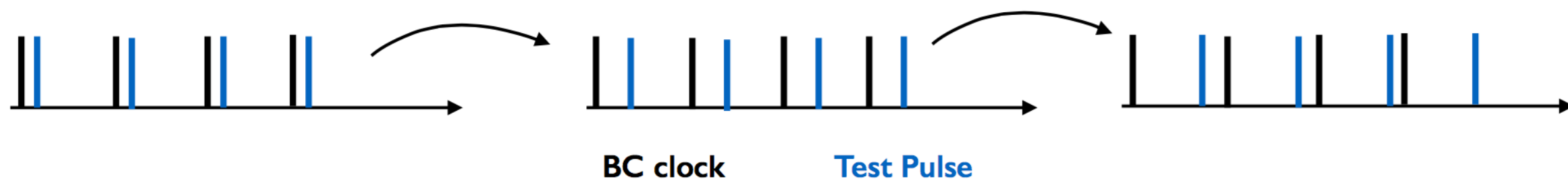
pedestals



There are two methods for timing calibration

CKTP (test pulse) skewing

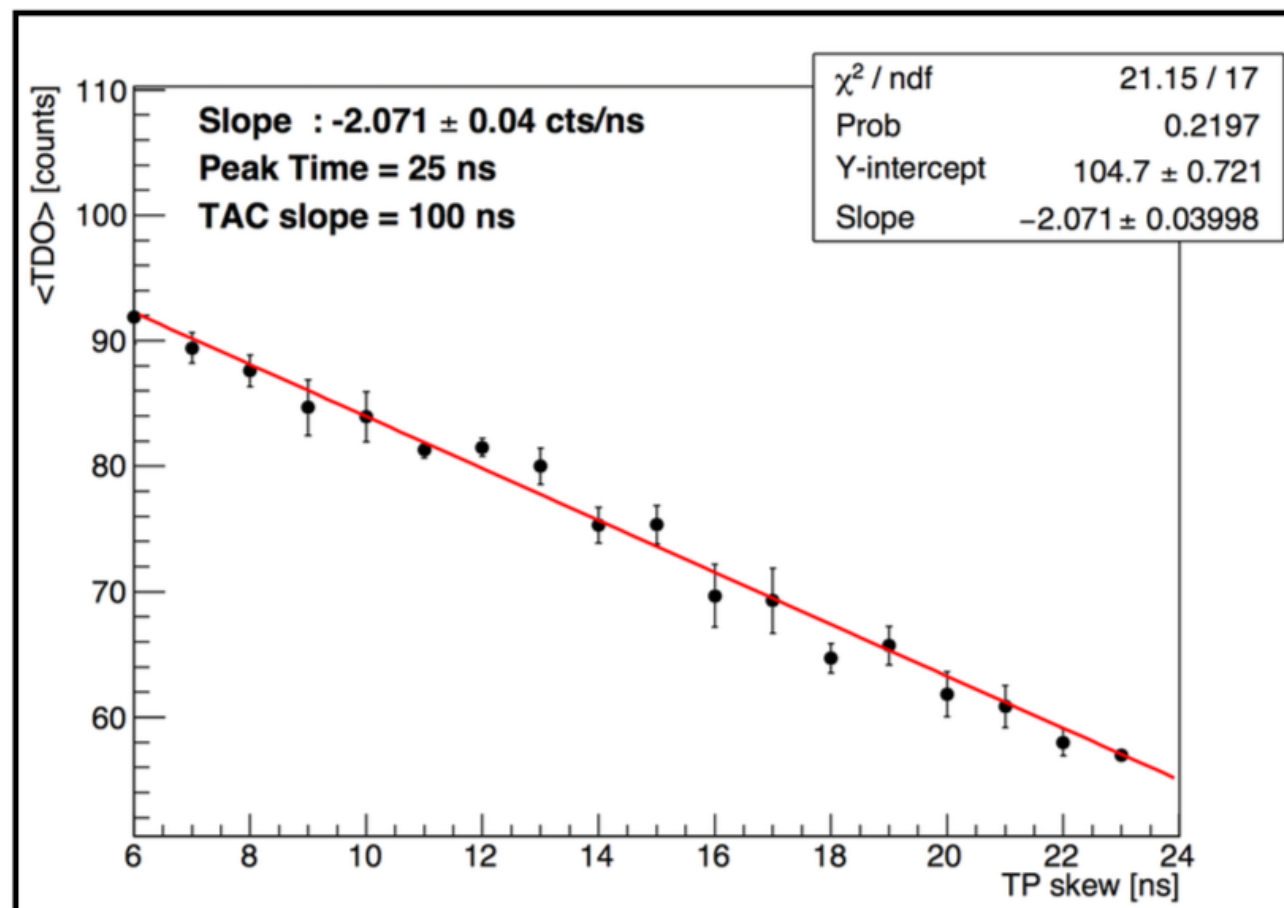
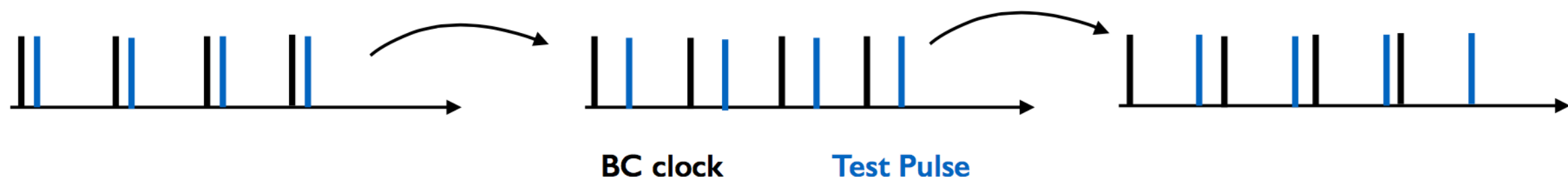
1. Skew the CKTP relative to CKBC in known time steps
2. From relation between TDO and known time delay, obtain conversion from TDO ADC counts to ns



There are two methods for timing calibration

CKTP (test pulse) skewing

1. Skew the CKTP relative to CKBC in known time steps
2. From relation between TDO and known time delay, obtain conversion from TDO ADC counts to ns



With this method:

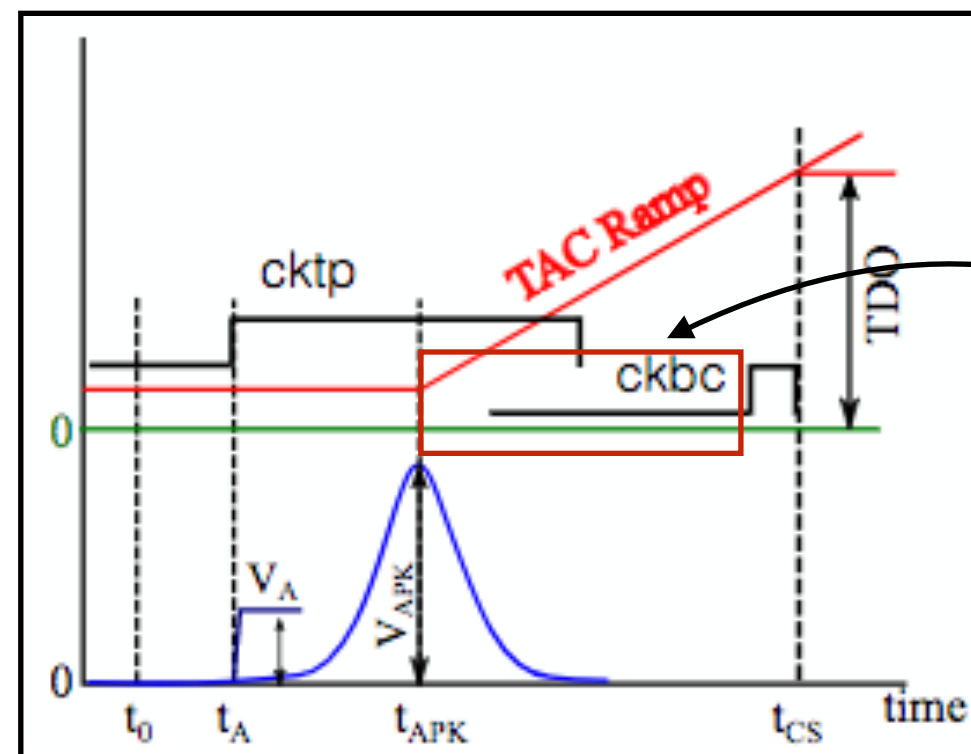
1. we cannot measure the full TDO range
2. we cannot measure any TDO pedestal
3. we have a limited number of sampling steps (CKTP skew constrained to be within time window of one BC — and first 3-5 cannot be used)

There are two methods for timing calibration

CKBC Latency Delays

1. Configure the VMM to be run in “Fixed Window” mode (i.e. *TAC ramp has a fixed latency*)
2. TAC ramp stops at next falling edge of CKBC after peak found — in “Fixed Window” mode we set CKBC low after signal crossing until the fixed latency is reached, and throw (a configurable # of) CKBC signals to stop the TAC
3. From relation between TDO and the known BC latency steps, obtain conversion between TDO and time as well as possible methods for TDO ADC pedestal measurement

we implemented the ability to do this after timing analysis begun on the test beam data

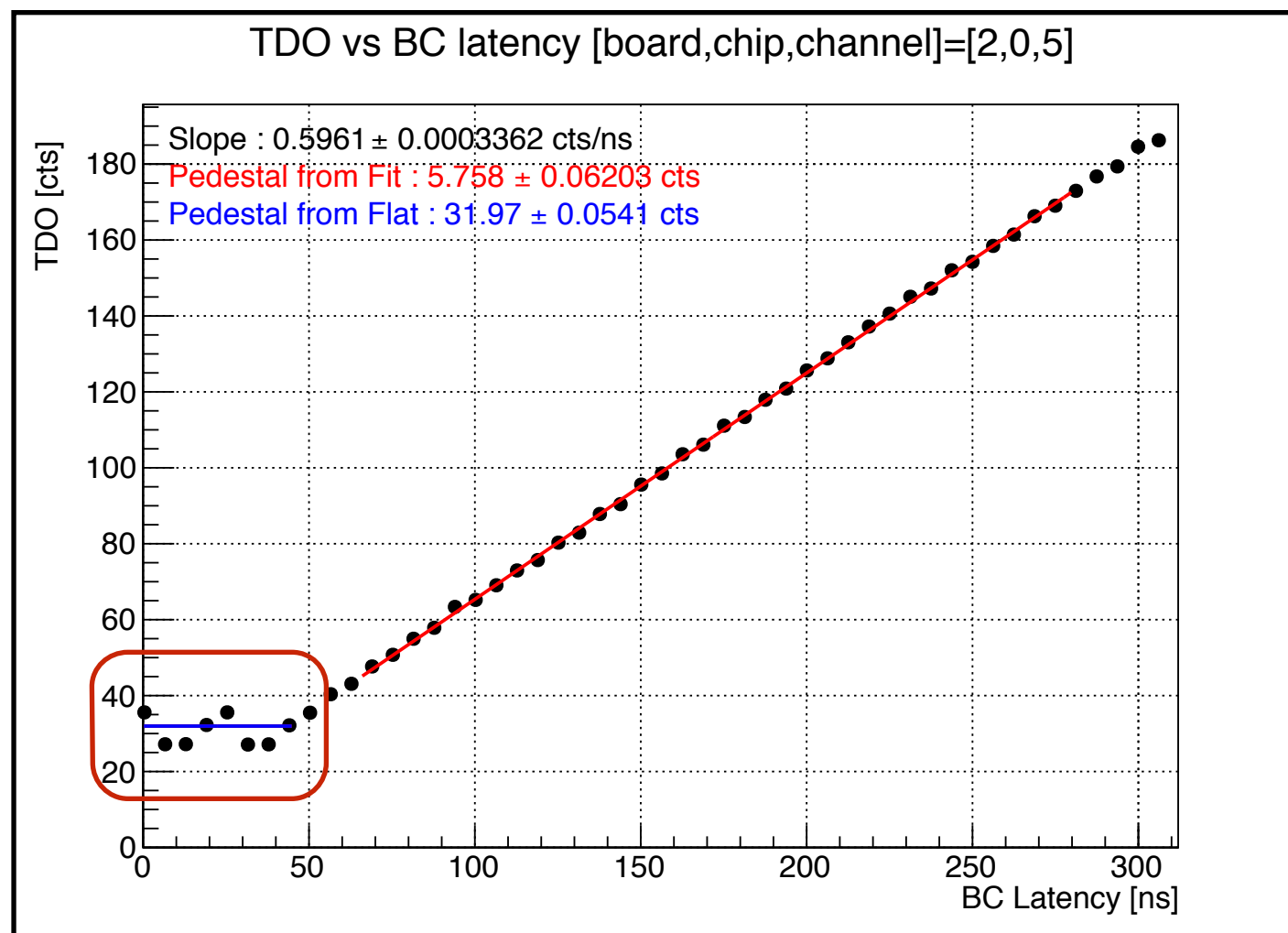


we adjust this window length

There are two methods for timing calibration

CKBC Latency Delays

1. Configure the VMM to be run in “Fixed Window” mode (i.e. *TAC ramp has a fixed latency*)
2. TAC ramp stops at next falling edge of CKBC after peak found — in “Fixed Window” mode we set CKBC low after signal crossing until the fixed latency is reached, and throw (a configurable # of) CKBC signals to stop the TAC
3. From relation between TDO and the known BC latency steps, obtain conversion between TDO and time as well as possible methods for TDO ADC pedestal measurement



With this method we can achieve many more (higher quality) measurements and can obtain a measure of the pedestal

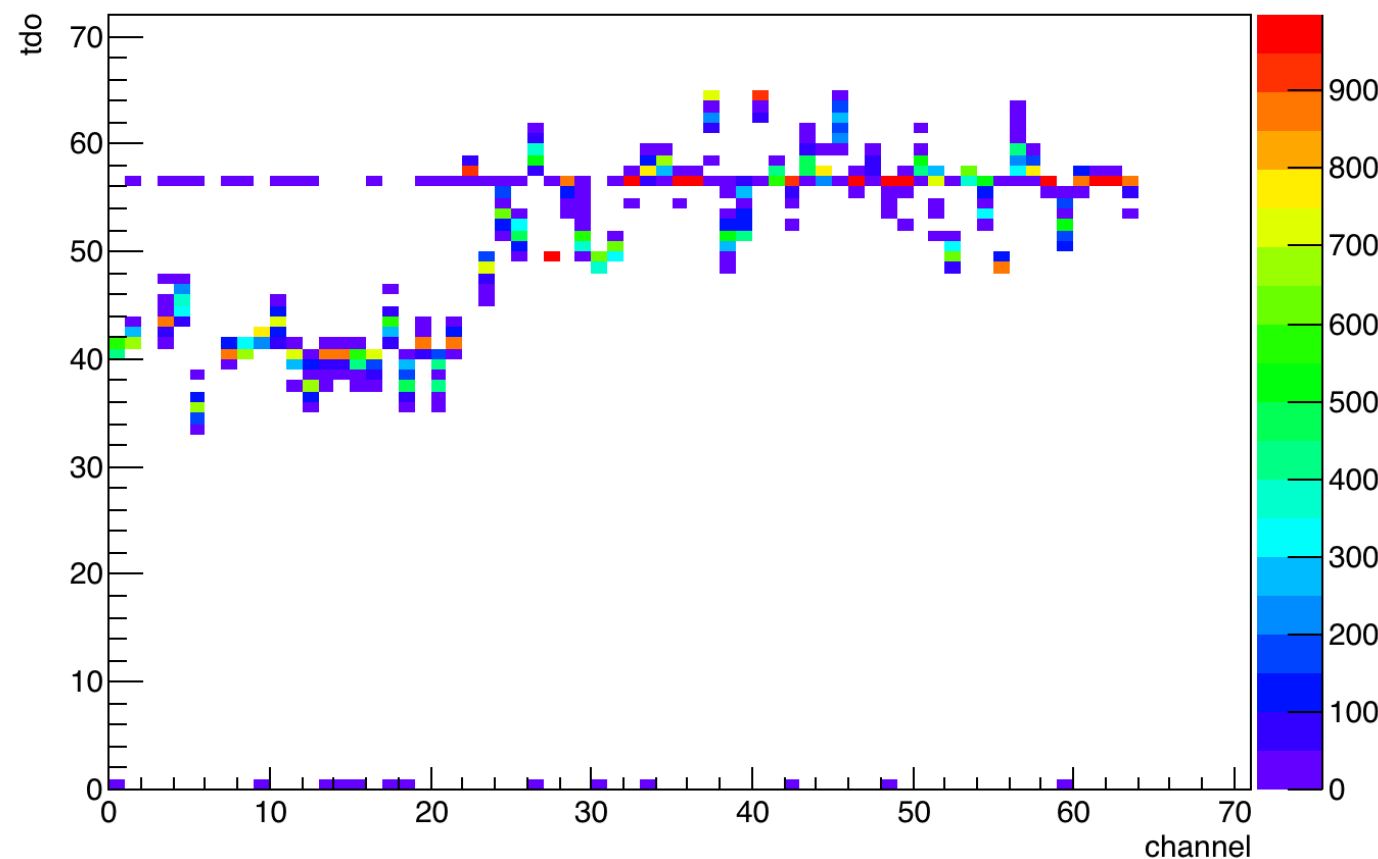
Two pedestal measures: y-intercept of linear fit and/or constant fit in “flat” region

There are two methods for timing calibration

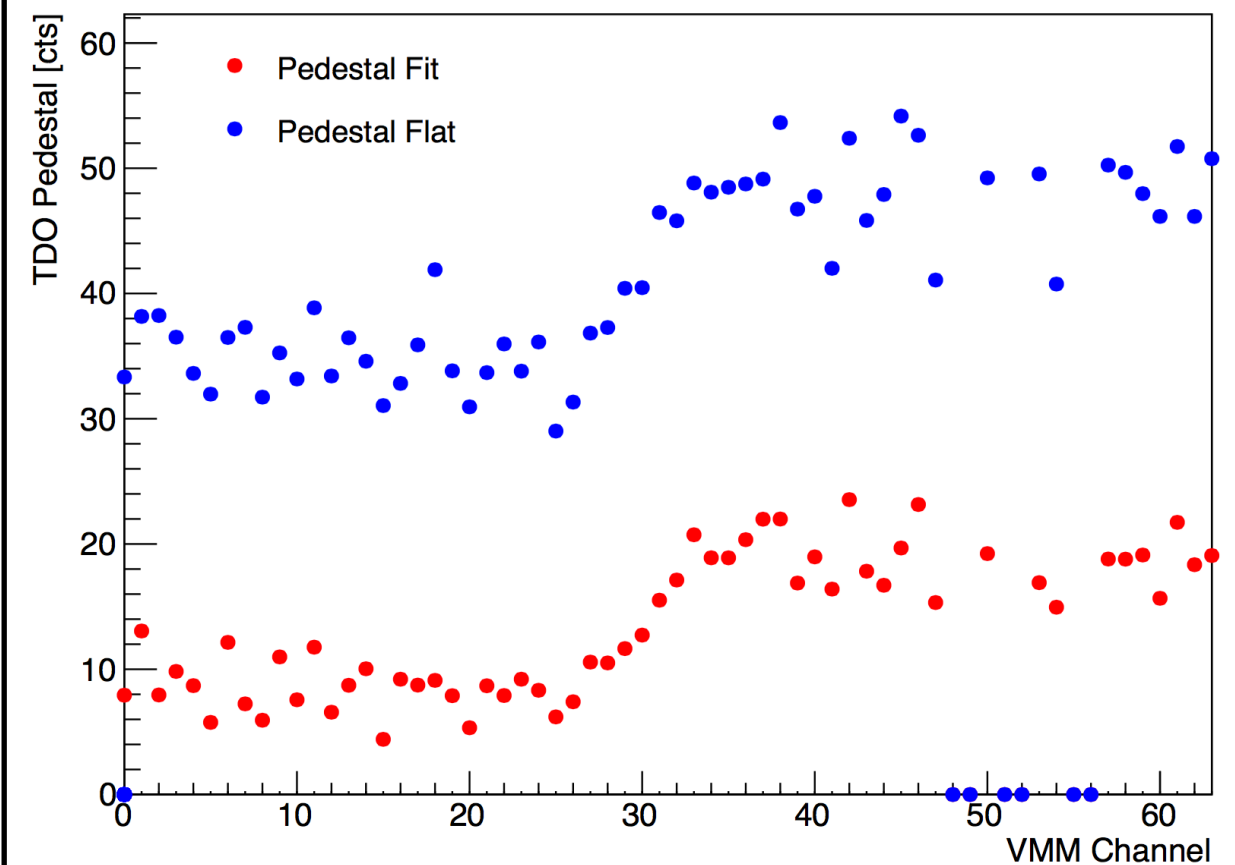
CKBC Latency Delays

Having the pedestal correction proved useful during the test beam analysis, where we saw channel-by-channel pedestal variations in the TDO

tdo:channel {pulserCounts==400}



TDO Pedestals for [board,chip]=[2,0]



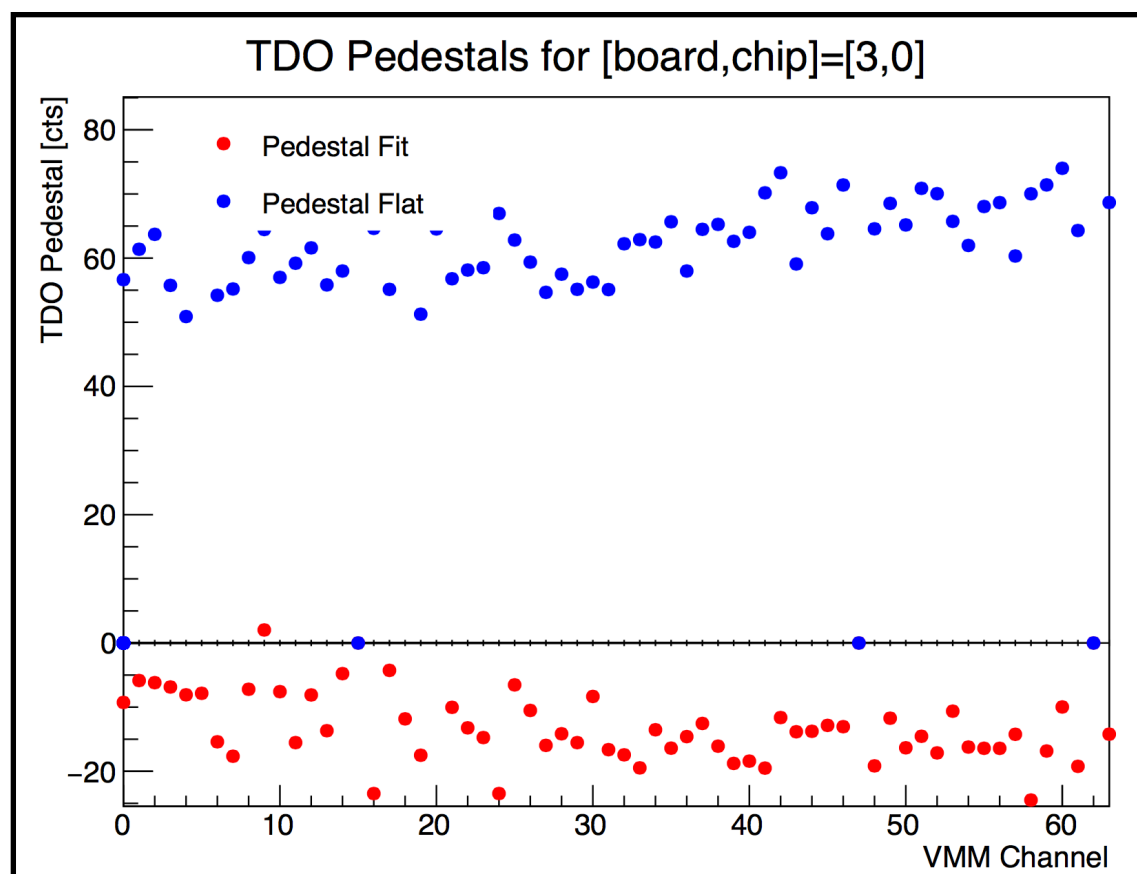
There are two methods for timing calibration

CKBC Latency Delays

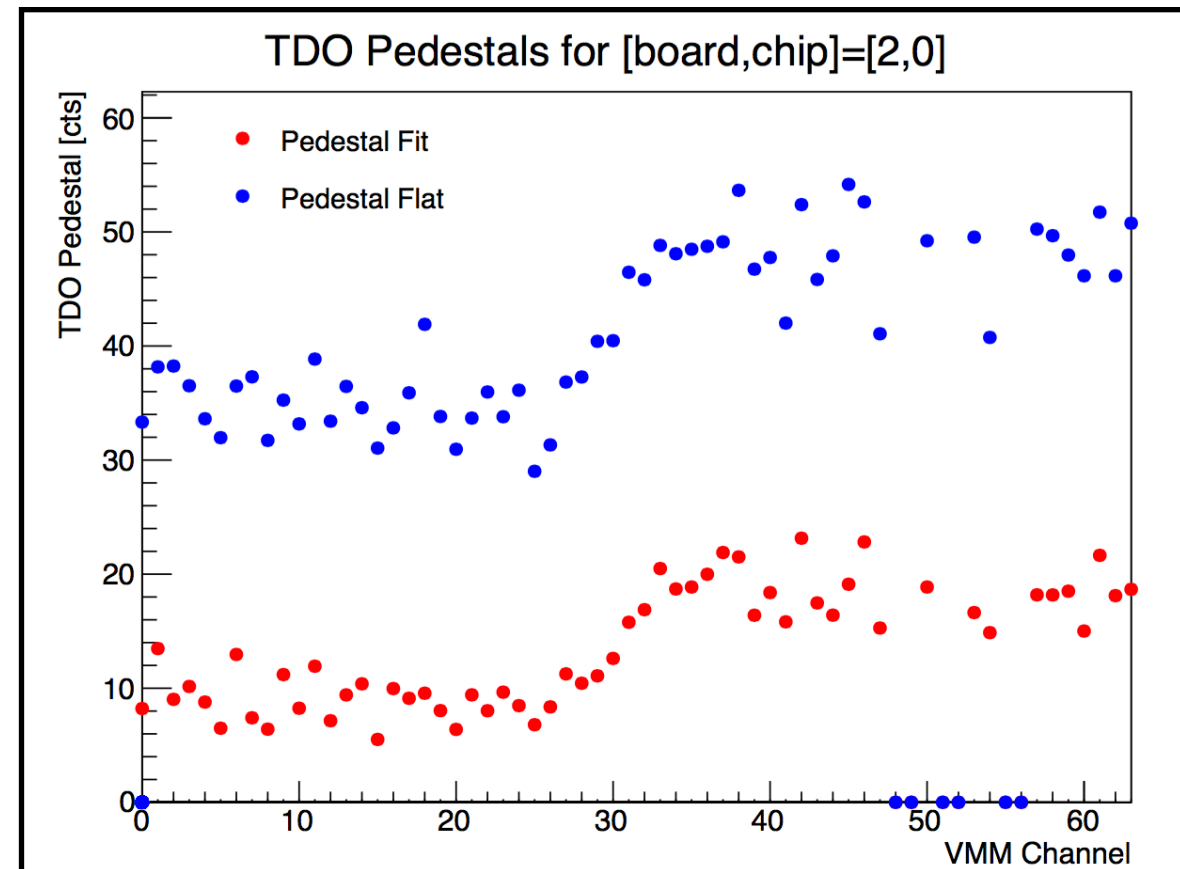
The conversion constants are different for different TAC slopes (of course)

We also saw/see dependence of the TDO pedestals on the TAC

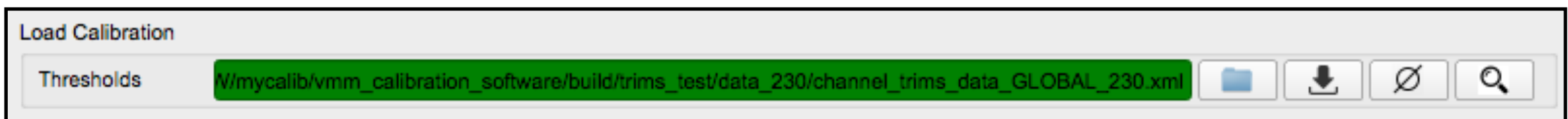
TAC = 100 ns



TAC = 350 ns



- All of these calibration analysis procedures are implemented in the software package [vmm_calibration_software/](#) (except for CKTP skewing timing calibration) and run on the calibration n-tuples produced by VERSO
- All of the plots (and more) shown here are produced in this package, as well as the calibration parameters being stored in text/XML for later use in analysis/data taking
 - e.g. Channel trimmer calibration can be loaded into VERSO and during VMM configuration, each VMM and board will be configured with its chosen & equalized trimmer settings
- Will work to incorporate the other calibration data (e.g. DAC + baseline calibration) into VERSO, though much is for off-line analysis



```
VERSO Info      Setting threshold calibration file to:
VERSO Info      /Users/dantrim/workarea/NSW/mycalib/vmm_calibration_software/build/trims_test/data_230/channel_trims_data_GLOBAL
VERSO Info      230.xml
VERSO Info      Loading threshold calibration
VERSO Info      Threshold calibration loaded successfully!
===== Loaded Threshold Settings =====
-----
BOARD IP: 192.168.0.2
  CHIP 7 | 0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
          | 23 16 13 27 20 10 31  6 30 30 31 17 13  0 16 12 18 31 31 20 13 19 18 31 27 16 30 26 12  3 16 31
          |-----|
          | 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
          | 30 14 31 24  0 14  5 23 31 31  4 23 31 10 21 25 10 28 31 16  0 31 24 27 31 25 12 31 16 21 29 25
          |-----|
=====
```