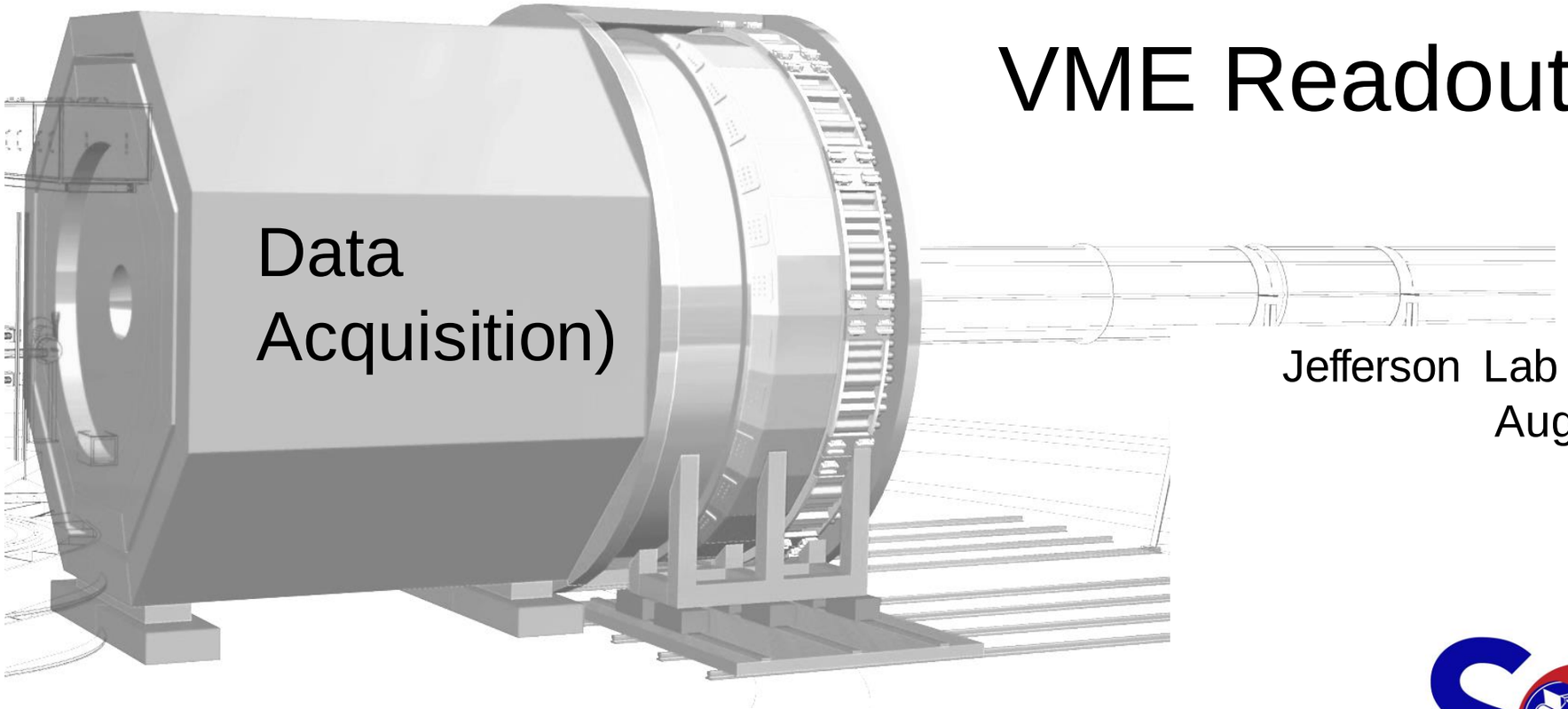

VME Readout Upgrade

Data Acquisition)

Jefferson Lab SoLID Pre-R&D Review
August 7th, 2020

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Jlab FEDAQ

Overview

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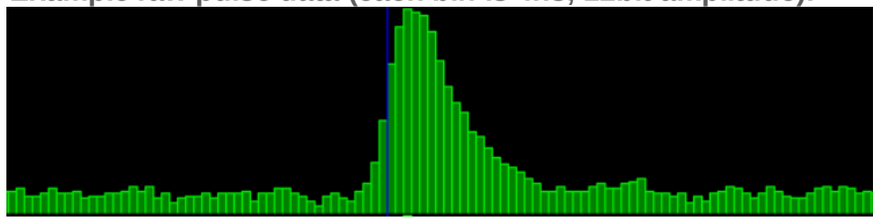
FADC250

FADC250

- 16 channels, 250Msps Flash ADC
- VME based module, supports 2eSST200 (200MByte/sec)
- Triggerable up to ~200kHz (depends on readout configuration/occupancy)
- VME data can provide raw pulse samples, or extracted charge/time (as well as scalers, pedestal data, and others)
- FADC250 has been used for >10 years at Jlab in many small to large experiments

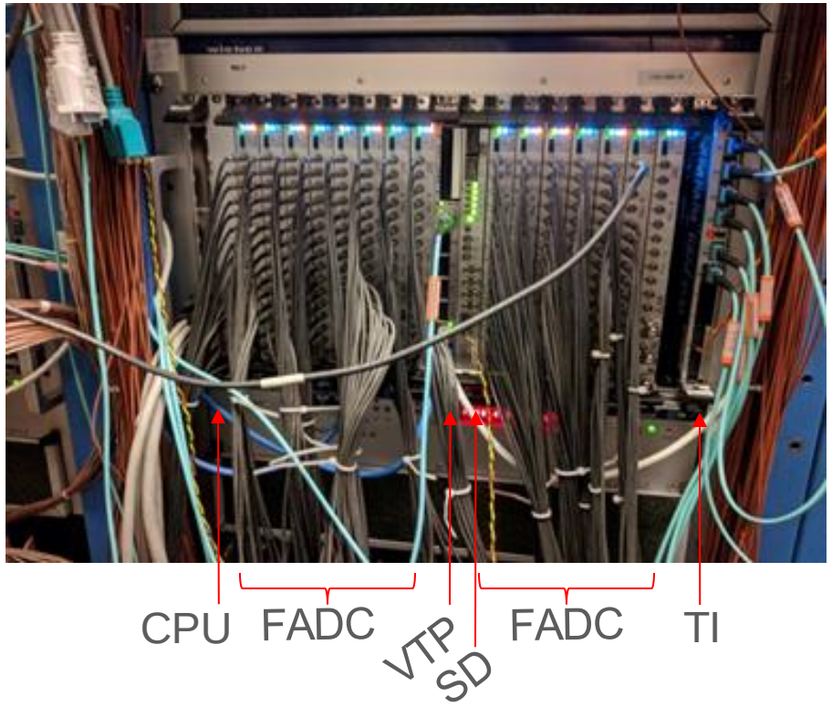
Example raw pulse data (each bin is 4ns, 12bit amplitude):



VXS Crate

- 21 slot VME crate, with VITA 41 VXS extension
- VXS allows us to distribute high quality point-to-point signals
  - Used for clock, trigger, etc. distribution on backplane
  - Also used for high speed serial communication – to be discussed later
- VME CPU in first slot manages the crate, reads out module data on trigger (or block of triggers), formats and ships data over ethernet
- VME readout mode used: 200MB/s, in practice we can get ~180MB/s, but often we are limited by the Ethernet
- CPU ethernet is typically 1Gbps, which limits data rate from crate to ~100MB/s. Adding a 10Gbps Ethernet card to CPU the ~180MB/s VME bandwidth is possible.

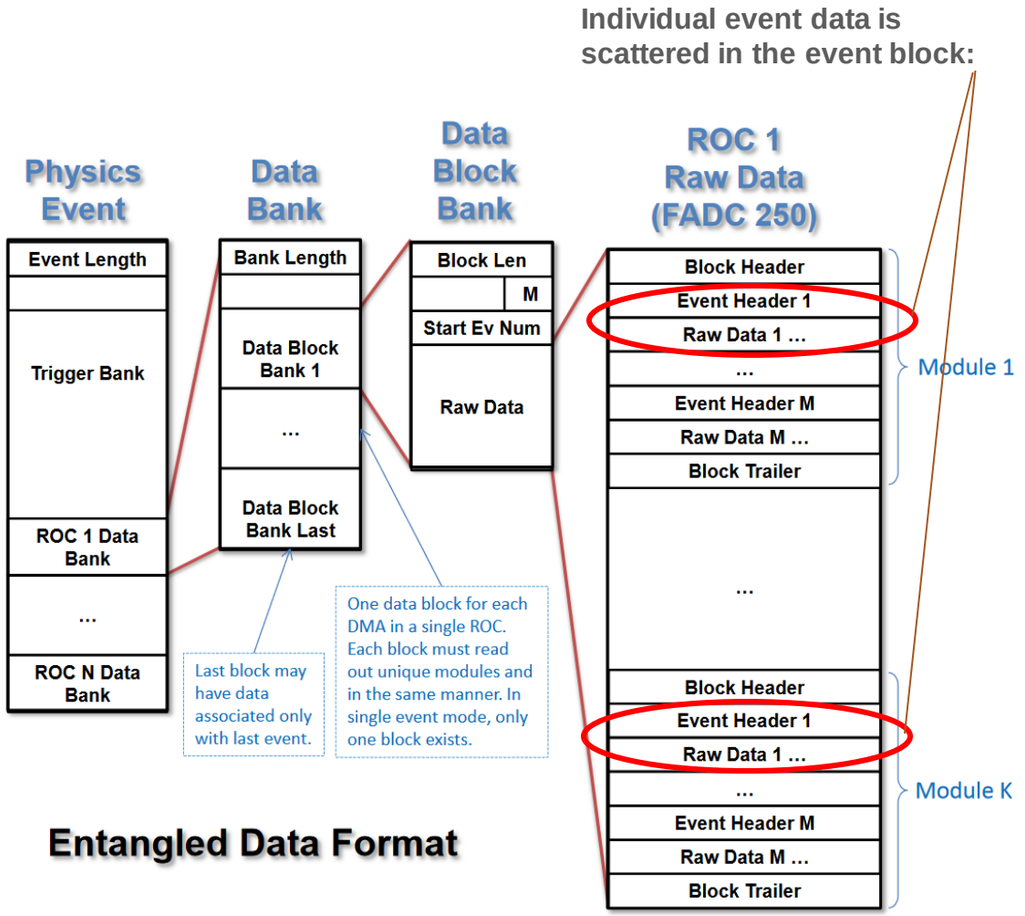
VXS Crate of FADC250 (256 channels)



- CPU: Intel/Linux
- FADC: Flash ADC 250MHz 16channels
- VTP: VXS Trigger Processor
- SD: Signal Distribution
- TI: Trigger Interface

Event blocking

- To reduce CPU & VME readout overhead, events are readout in "blocks" of events
  - Typically events are readout in blocks of 20 or 40 events
  - Trigger rates >100kHz can be achieved with low dead-time in this way – otherwise ~10kHz is the non-event blocking limit
- This complicates the data structure because now single events are "entangled" (i.e. spread across the data record), making offline data processing a bit of an annoyance

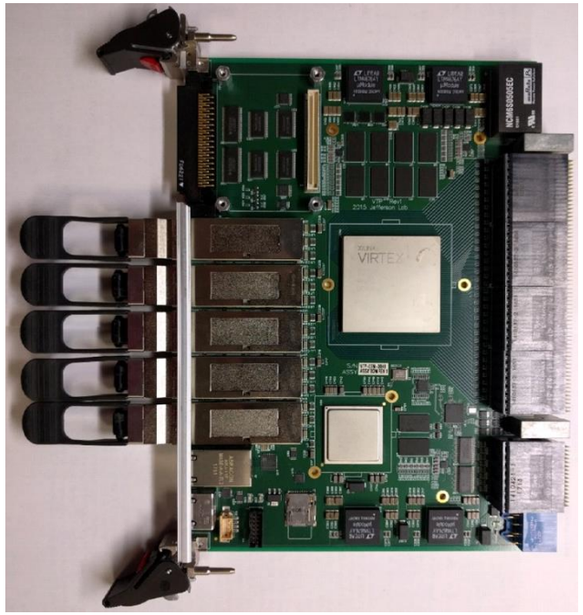


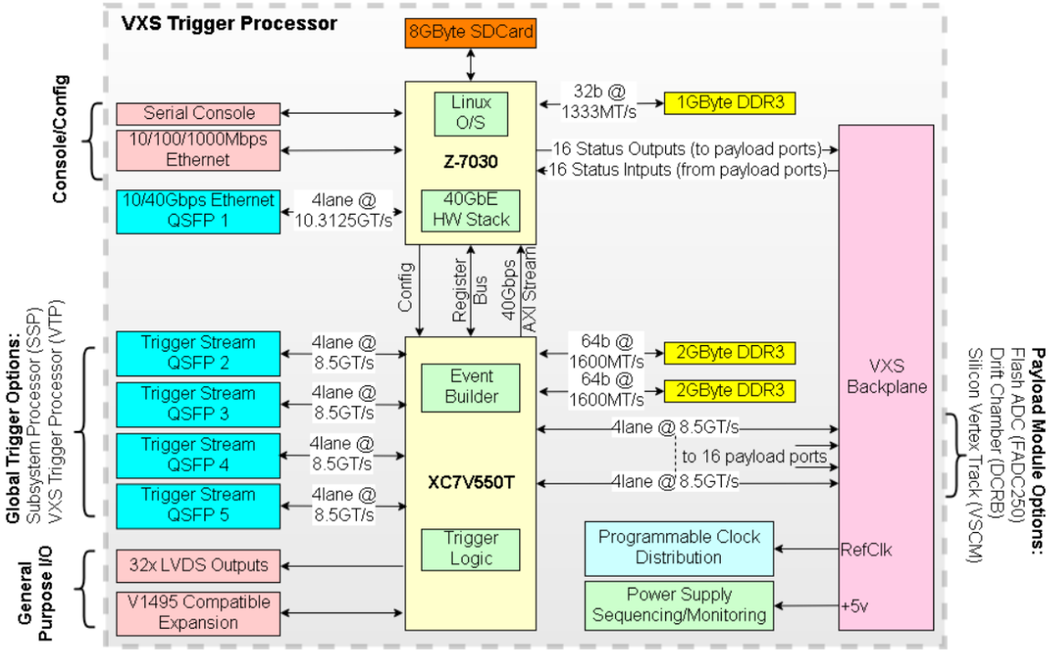
VXS Based Trigger

VTP (VXS Trigger Processor)

- Used in the crate when a trigger needs to be formed from the FADC250 (and/or other Jlab modules) - up to 16 FADC250 modules send trigger data to the VTP
- Each FADC250 in the VXS crate is connected to the VTP with 4 full duplex serial links that can operate up to 6.25Gbps each
- The trigger requires 10Gbps of bandwidth from each FADC -> VTP, so normally runs 4 serial links at 2.5Gbps

VTP:



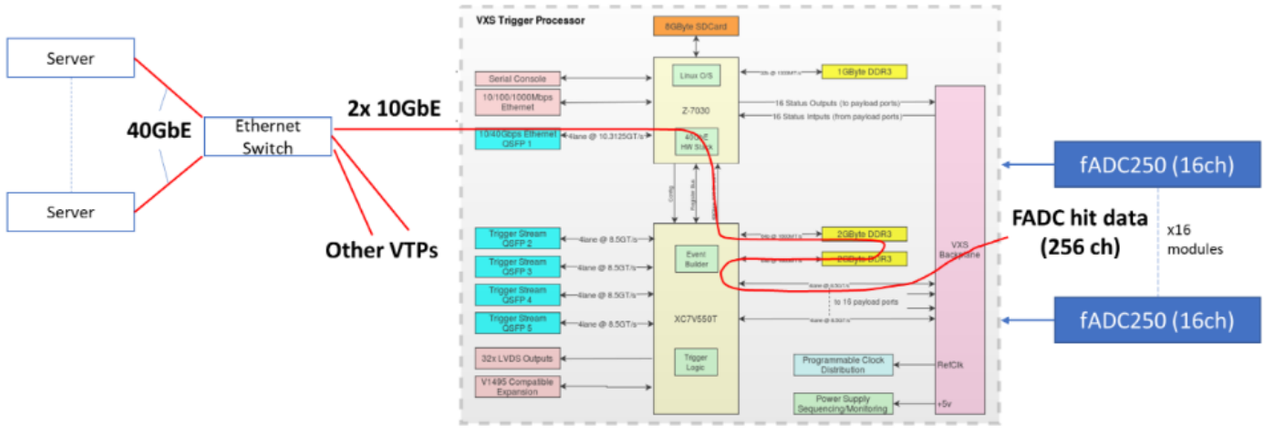


Streaming DAQ

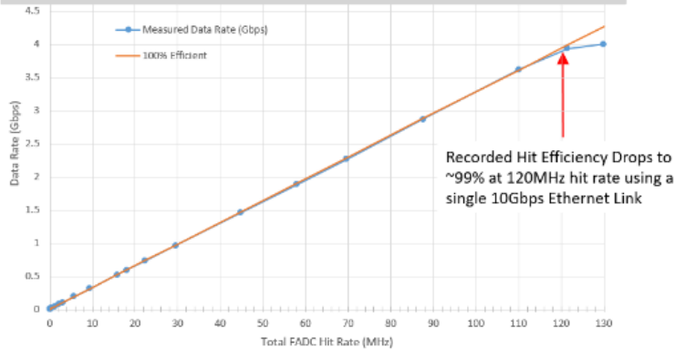
VTP + FADC250 has recently been used in a Streaming DAQ project where VTP collects hits from all FADC250 in crate and streams it over multiple 10Gbps Ethernet links using TCP. Several firmware components are re-usable which is a significant help.

Front-end setup 2 VXS crates, each with VTP w/ 2x 10GbE optical links, 11 FADC250 modules, 336 PbWO crystals w/APD

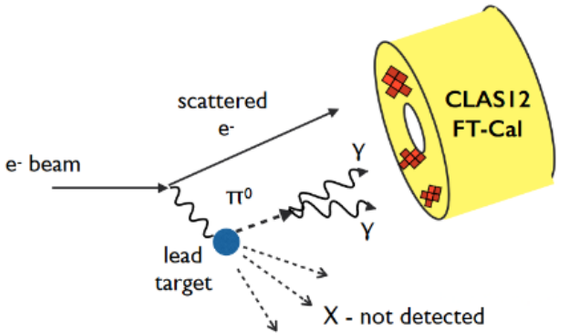
Backend setup servers connected to front-end ethernet switch by 40GbE. Combination of CODA, TRIDAS (by INFN), JANA2, ROOT for configuration, event selection, event reconstruction, and online monitoring

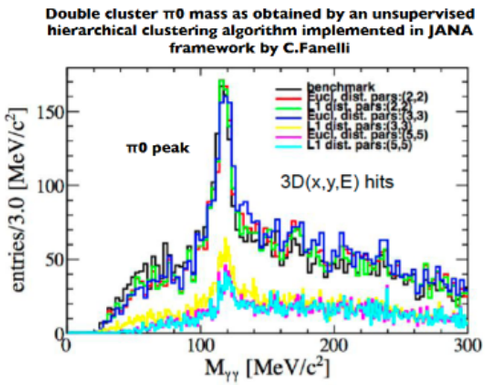


Rate capability Close to 1MHz rate per FADC channel before suffering efficiency loss (nearly 2x better after recent bandwidth improvements)



π^0 reconstructed signal from streaming readout rest



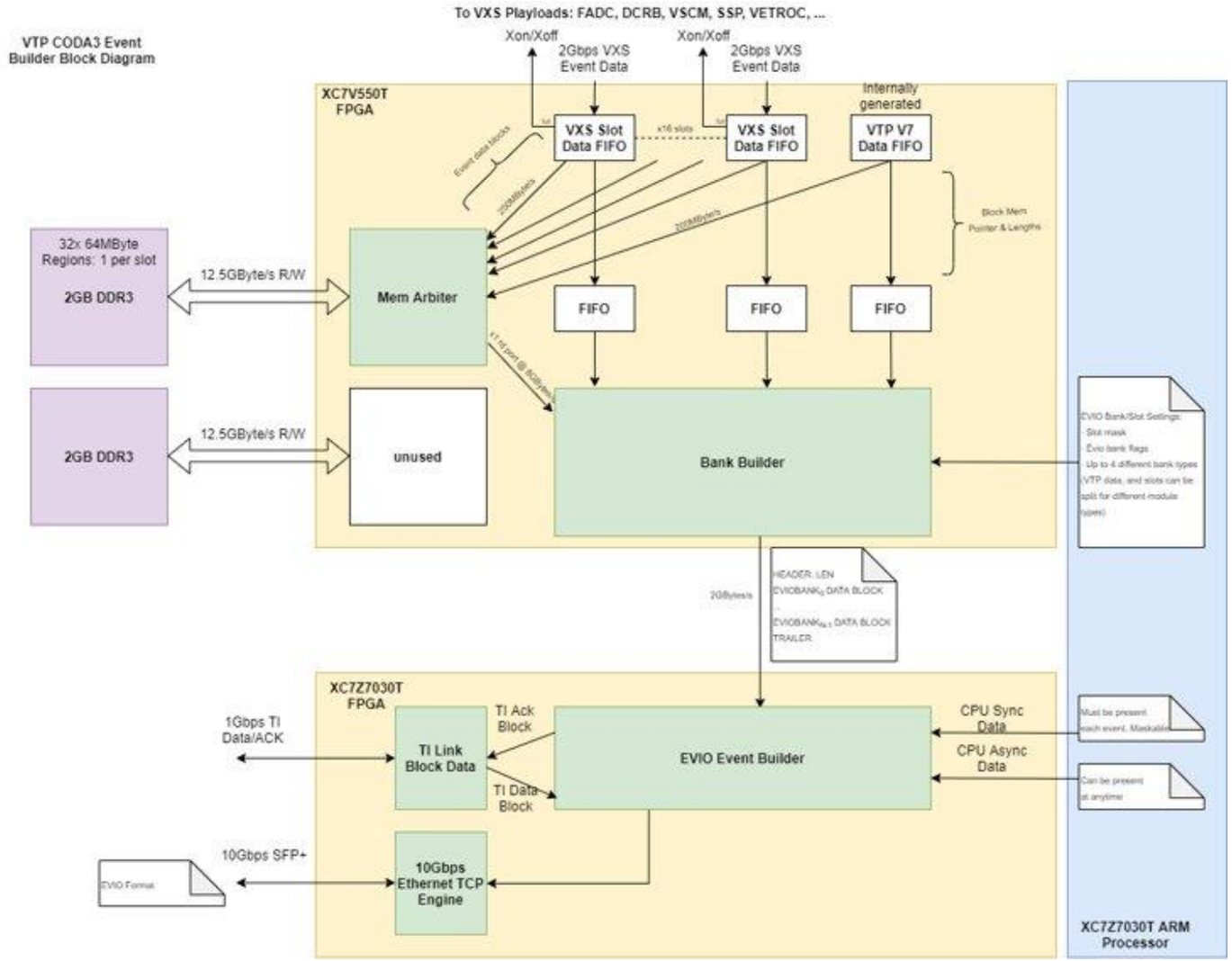


VXS Readout with VTP

- Increasing the FADC250 -> VTP serial link will allow sending both trigger and readout data over the same link:
  - Current 4 lanes at 2.5Gbps provide 10Gbps for the trigger
  - Changing to 4 lanes at 3.125Gbps will be enough for trigger + **200MB/s of event readout bandwidth from each FADC250** to the VTP – this is significantly more than the VME 200MB/s limit which is for the whole backplane
- VTP has 4 free 10Gbps compatible Ethernet optical links available for transmitting event data onto the network. Currently only a single 10Gbps link is planned to be used. **Nearly the full link 10Gbps link speed can be utilized for event data transport.**
- All event building, Ethernet, and TCP/IP is done in the FPGA and there is no significant overhead associate with individual events – this means **no event block is needed to support high trigger rates**.

VTP CODA3 Block Diagram

- Firmware will be fully compliant with CODA3 event builder: downstream components won't know the difference.
- VTP has large memory buffers to hold event data from individual modules (64MB per module)
- The CPU on the VTP will run a readout list – it can optionally participate event-by-event, but the main difference between this readout list and the traditional VME CPU readout list is that all VME module data will be handled in firmware.
- This is a generic implementation that can support other Jlab modules besides the FADC250 (e.g. DCRB, VSCM, SSP, VETROC) - other experiments besides SoLID can benefit from this development.



Expected readout rate estimates/limits

SoLID experiment configurations:
occupancy, trigger rate, data rate,
FADC readout mode/window

Status & Conclusion

- No new hardware is needed to support this upgraded readout mode (other than the typical crate configuration found at Jlab)
- FADC250 Firmware changes were small and completed (still need testing)
- VTP Firmware is still under development, but much already completed. Testing is expected to happen at the end of this summer/Fall.
- We have CODA experts involved (Dave Abbott, and Bryan Moffit) that will be helping to integrate, test, and ensure compatibility to make it easy for other experiments at Jlab to take advantage of this readout system upgrade.